



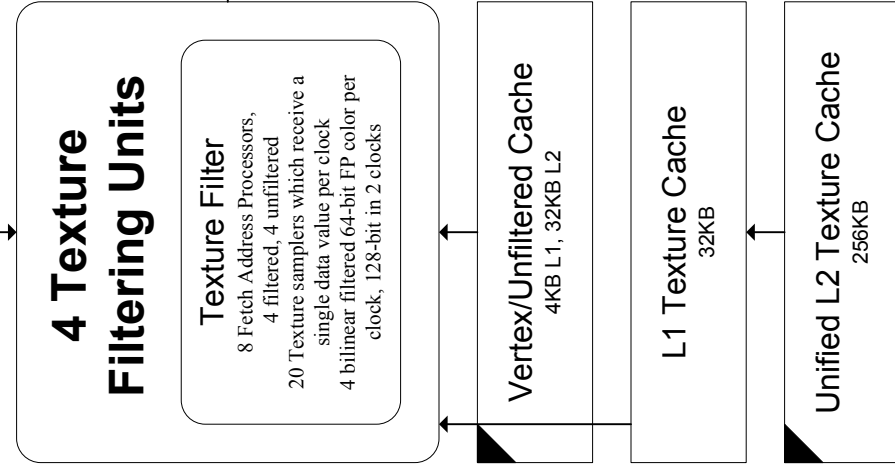
RADEON 2900



Legend: Read From Memory
Write To Memory
Memory Unit
Logic Unit

GNU/Linux Friendly
742 MHz
700 million transistors
420mm (20mmx21mm)
TSMC 80nm HS
~215Watts
475 GigaFLOPS
47.5 GigaPixel/s
742 Mtri/s
106 GB/s Memory Bandwidth
512 bit stacked I/O Memory Interface

Hierarchical Z and Stencil



Command Processor

RISC based Micro-Coded engine
Manages and distributes state throughout GPU

Vertex Assembler

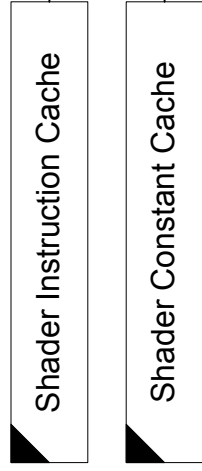
Primitive tessellation
Indices and instancing input values
Vertex addresses sent to shader core

Geometry Assembler

Uses on/off chip staging
Sends processed vertex addresses, near neighbor addresses and topological information to shader core

Rasterizer Interpolators

Triangle setup
Interfaces to depth for HiZ/EarlyZ results



Thread Dispatcher

Thread arbiter and sequencers for each SIMD, Texture and Vertex Fetch

All threads have 64 elements
100's of threads in flight

Threads are put to sleep when they request a slow responding resource
Arbitration policy is a programmable combination of factors which include age, need, and availability.

320 Stream Processing Units

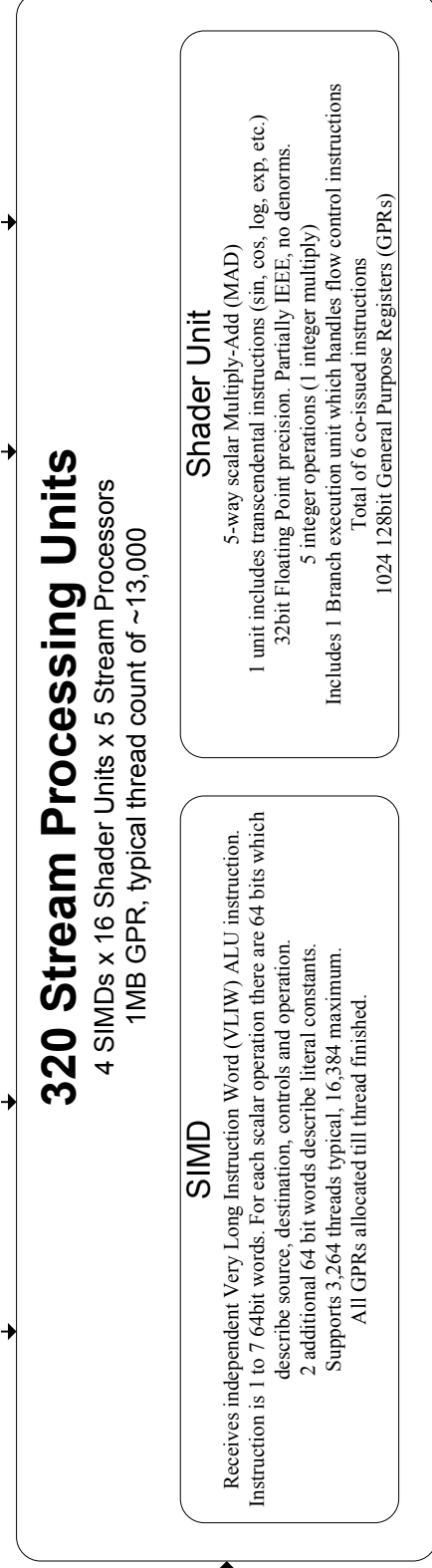
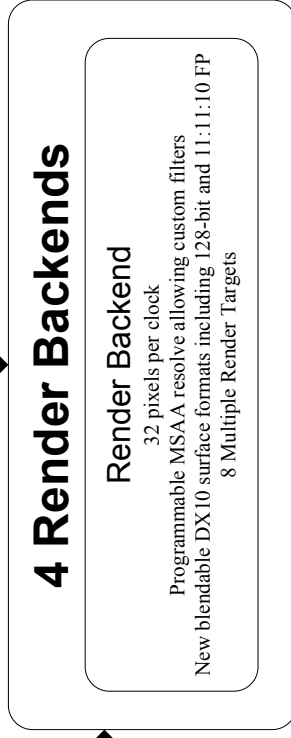
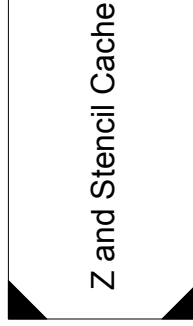
4 SIMDs x 16 Shader Units x 5 Stream Processors
1MB GPR, typical thread count of ~13,000

SIMD
Receives independent Very Long Instruction Word (VLW) ALU instruction. Instruction is 1 to 7 64bit words. For each scalar operation there are 64 bits which describe source, destination, controls and operation.
2 additional 64 bit words describe literal constants.
Supports 3,264 threads typical, 16,384 maximum.
All GPRs allocated till thread finished.

Shader Unit
5-way scalar Multiply-Add (MAD)
1 unit includes transcendental instructions (sin, cos, log, exp, etc.)
32bit Floating Point precision. Partially IEEE, no denorms.
5 integer operations (1 integer multiply)
Includes 1 Branch execution unit which handles flow control instructions
Total of 6 co-issued instructions
1024 128bit General Purpose Registers (GPRs)



Shader Export



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