



ATI Radeon™ 4800 series Graphics

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Graphics Product Group



Graphics Processing Units

- ATI Radeon™ HD 4870
- AMD Stream Computing
- Next Generation GPUs



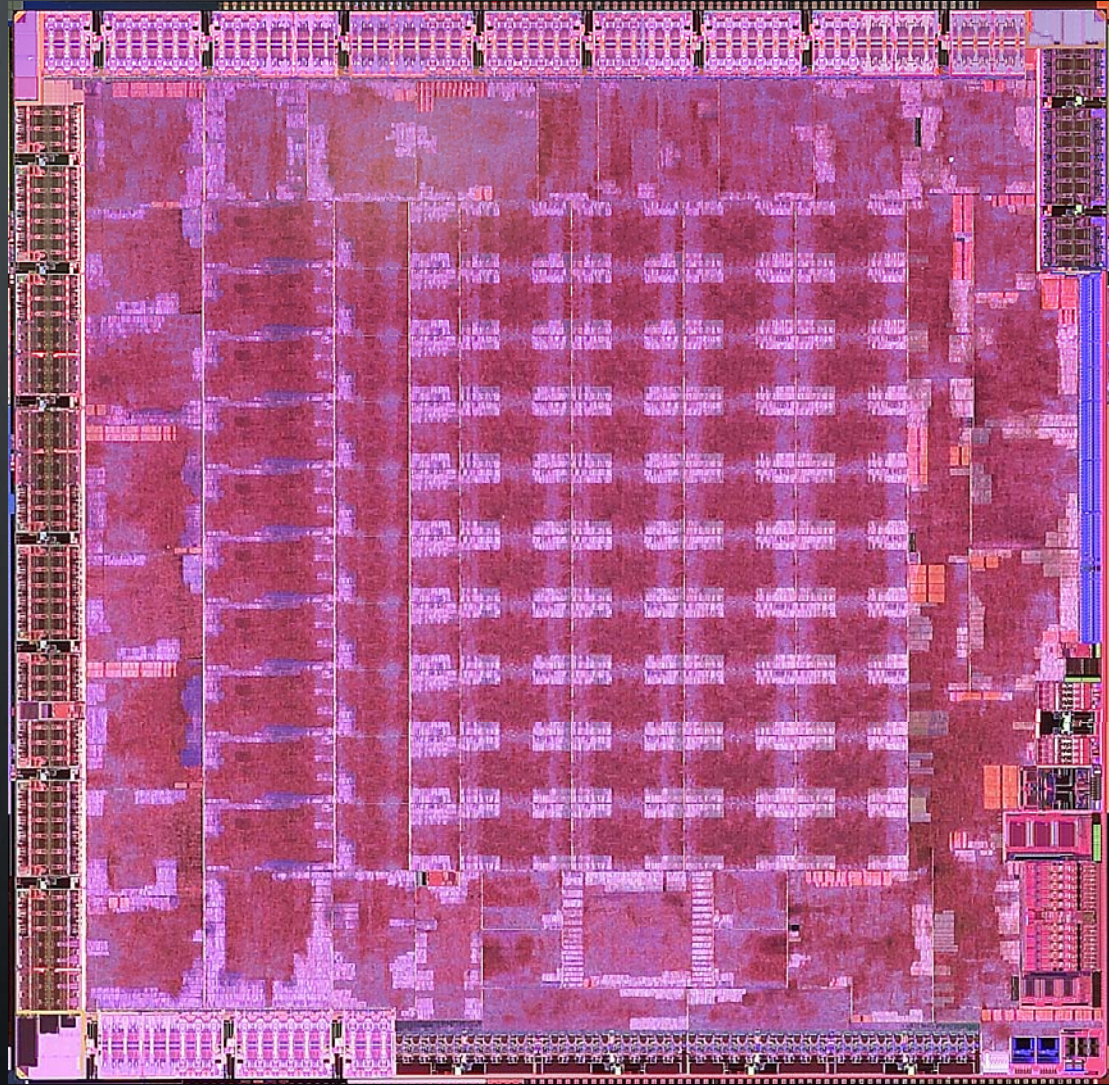
ATI Radeon™ HD 4800 Series

- Performance per watt/mm²/dollar
- ATI Radeon™ HD 4870
 - USD\$299 (MSRP)
 - 1.2 teraFLOPS
 - Core clock 750 MHz
 - 512 MB of GDDR5 - 3.6 gigabits/s
 - dual-slot PCI Express 2.0
 - 160 watts (TDP)
- ATI Radeon™ HD 4850
 - USD\$199 (MSRP)
 - 1 teraFLOP
 - Core clock 625 MHz
 - 512 MB of GDDR3 - 2 gigabits/s
 - single-slot PCI Express 2.0
 - 110 watts (TDP)



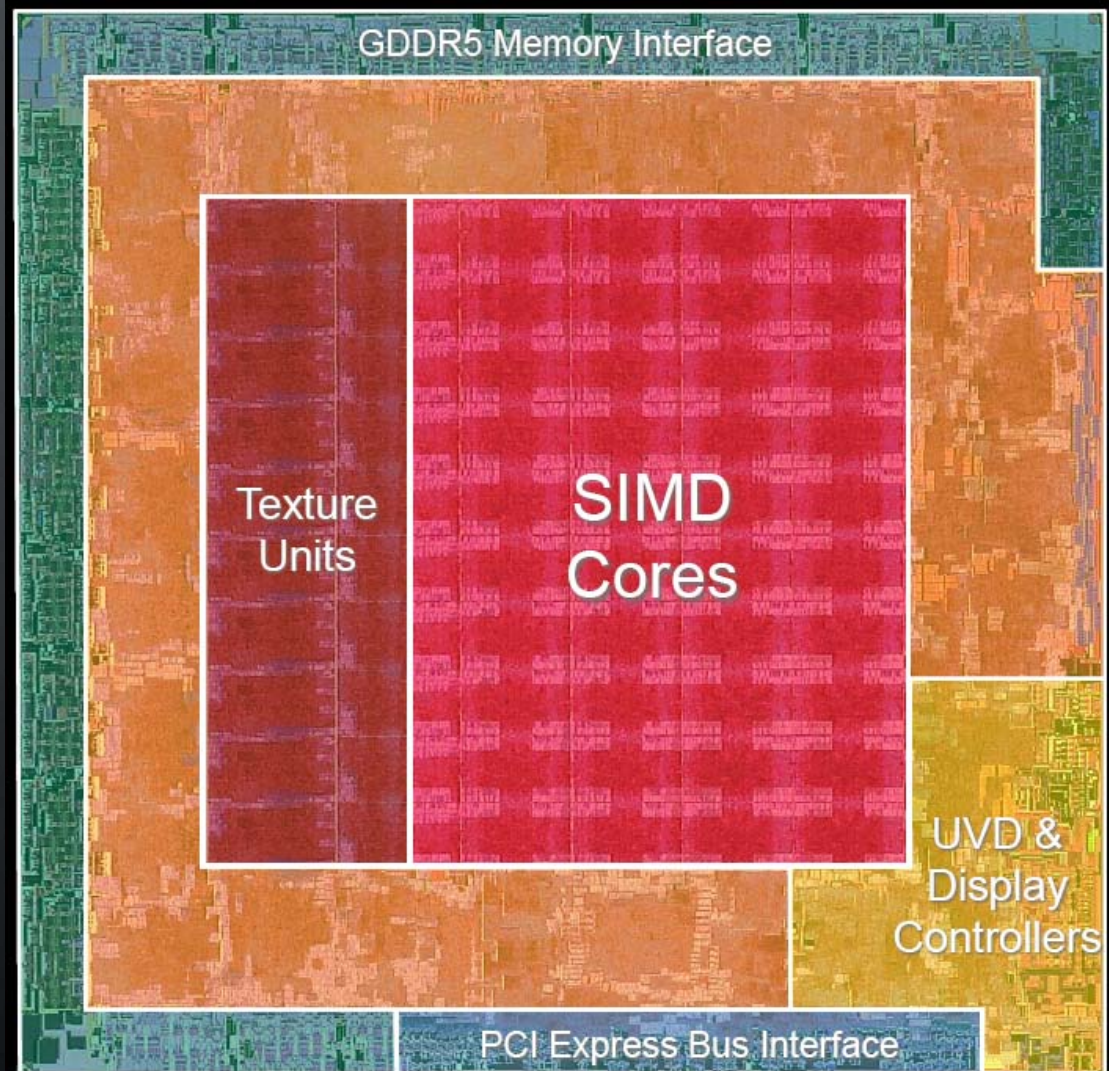
ATI Radeon™ HD 4800 Series

- 260mm²
- 956 MTransistors
- 64 z/stencil
- 40 texture
- 10 SIMDs
 - 800 shaders



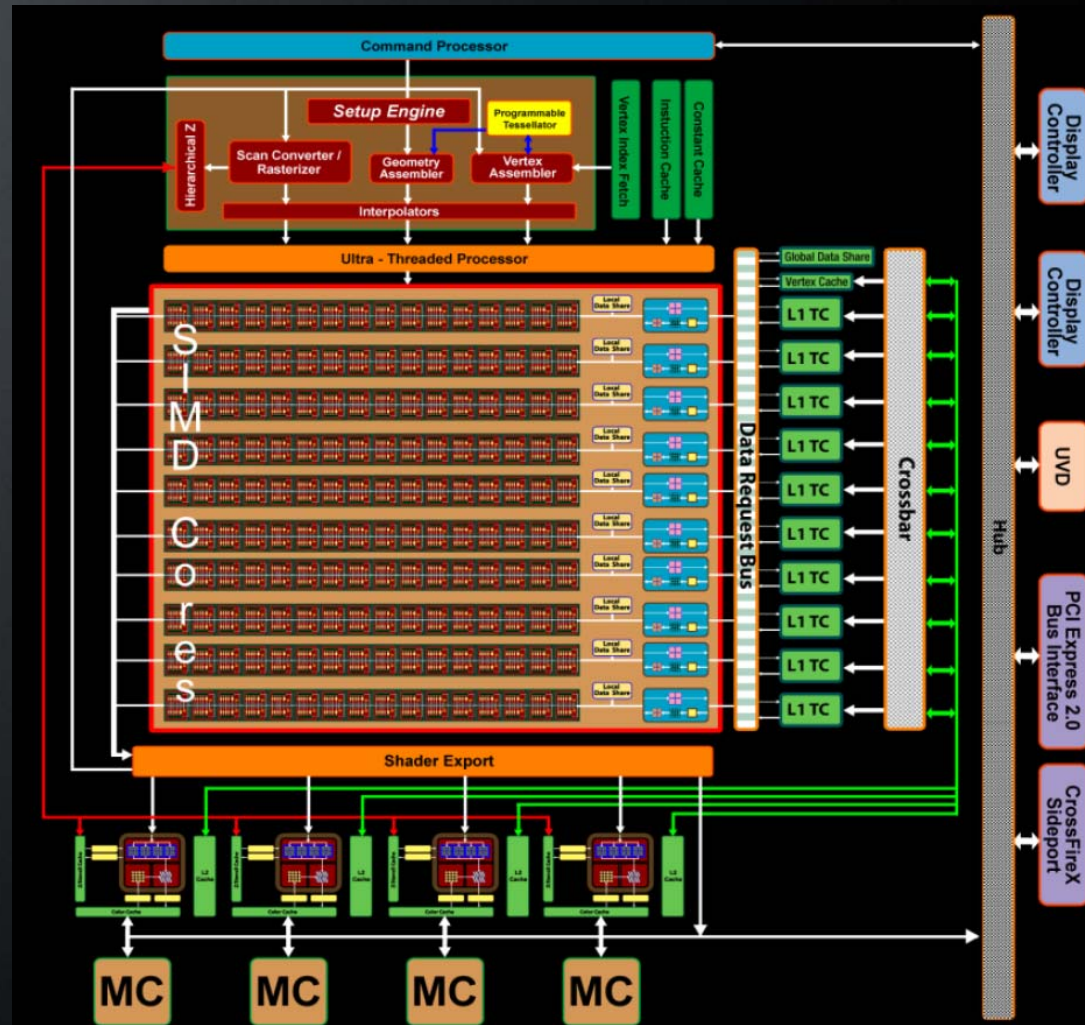
ATI Radeon™ HD 4800 Series

- 260mm²
- 956 MTransistors
- 64 z/stencil
- 40 texture
- 10 SIMDs
 - 80 32bit FP Stream Processing Units (SPUs)



ATI Radeon™ 4800 Series Architecture

- 800 stream processing units
- New SIMD core layout
- New texture cache design
- New memory architecture
- Optimized texture and render back-ends
- Enhanced geometry shader



SIMD Cores

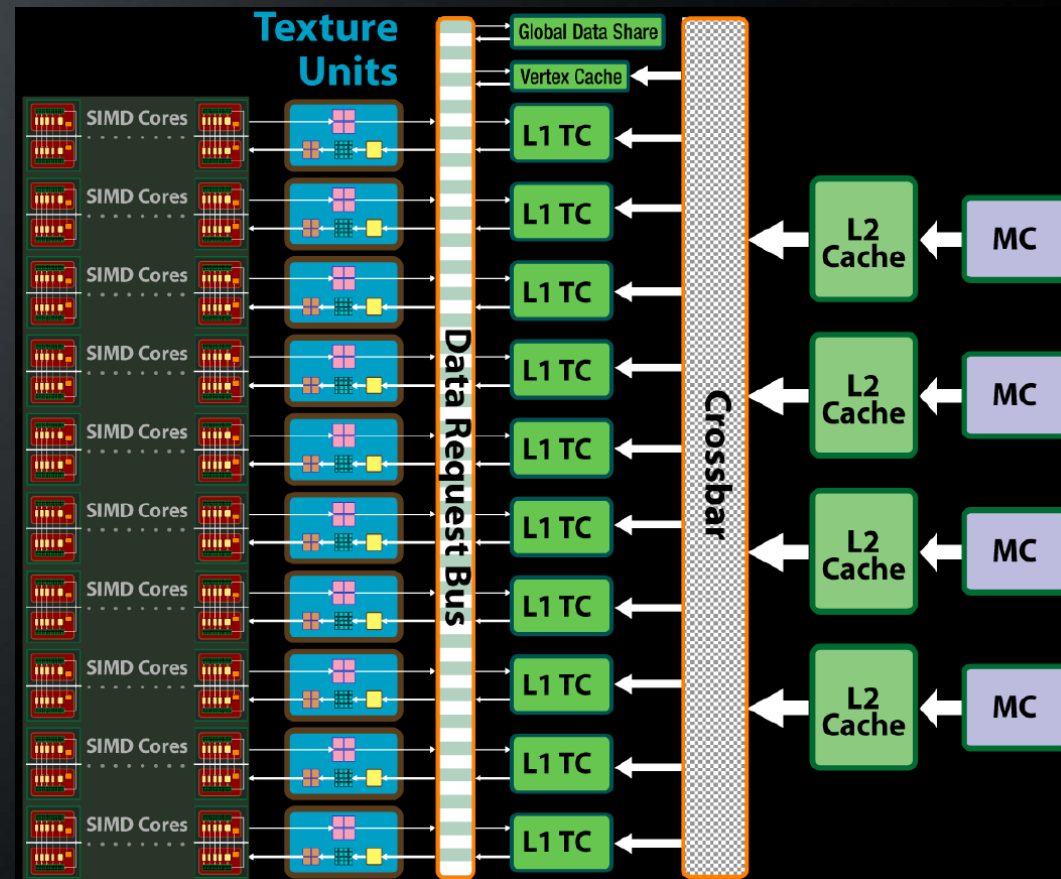
- Each core:
 - Includes 80 scalar stream processing units in total
 - 16KB Local Data Share
 - Persistent allocation of data between wavefronts
 - Has its own control logic and runs from a shared set of threads
 - Has 4 dedicated texture units + L1 cache
 - Communicates with other SIMD cores via 16KB Global Data Share
 - Data sharing between threads running on different SIMDs
- New design allows texture fetch capability to scale with shader power, maintaining 4:1 ALU:TEX ratio



Texture Units

New cache design

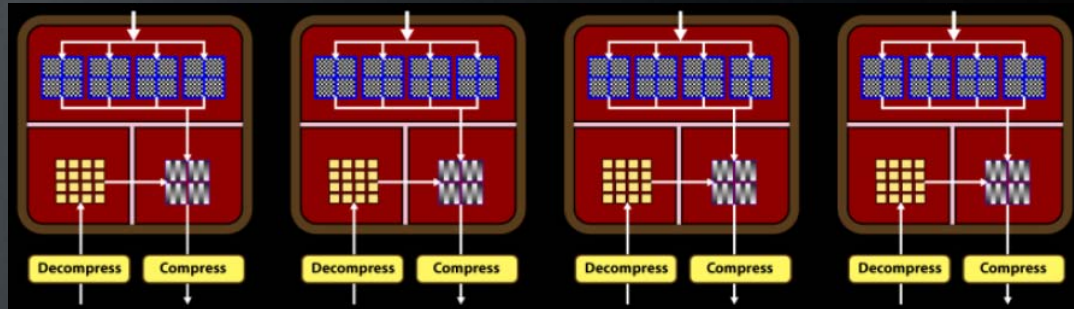
- L2s aligned with memory channels
- L1s store unique data per SIMD
 - 2x increase in effective storage per L1*
 - 5x increase overall*
- Separate vertex cache
- Increased bandwidth
 - Up to 480 GB/sec of L1 texture fetch bandwidth
 - Up to 384 GB/sec between L1 & L2



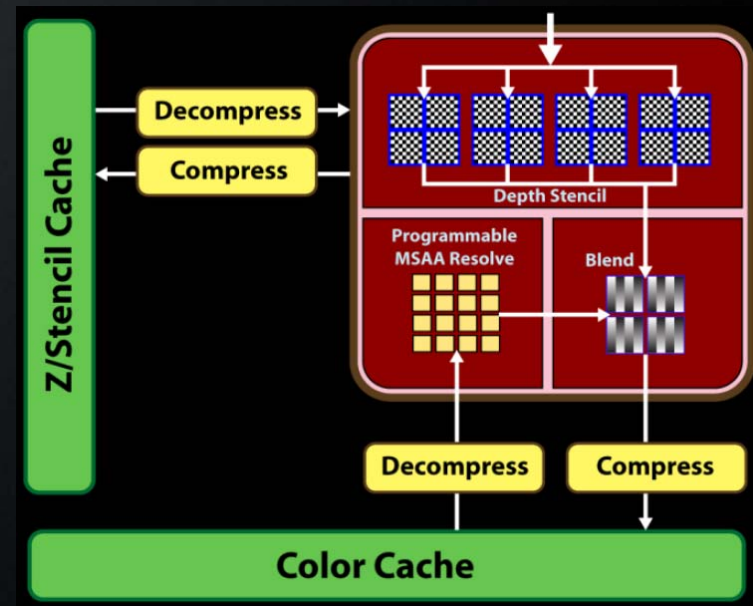
*compared to ATI Radeon™ 3870



Render Back-Ends

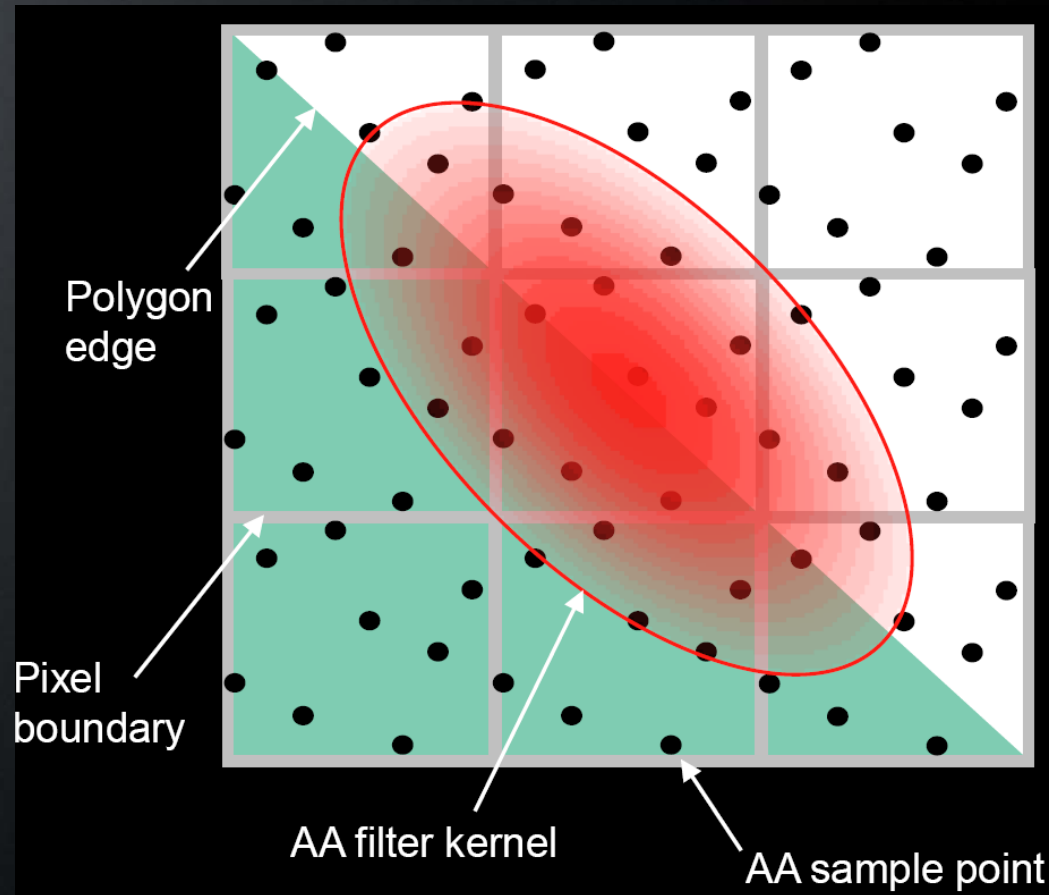


- Focus on improving AA performance per mm2
 - Doubled peak rate for depth/stencil ops to 64 per clock
 - Doubled AA fill rate for 32-bit & 64-bit color
 - Doubled non-AA fill rate for 64-bit color
- Supports both fixed function (MSAA) and programmable (CFAA) modes



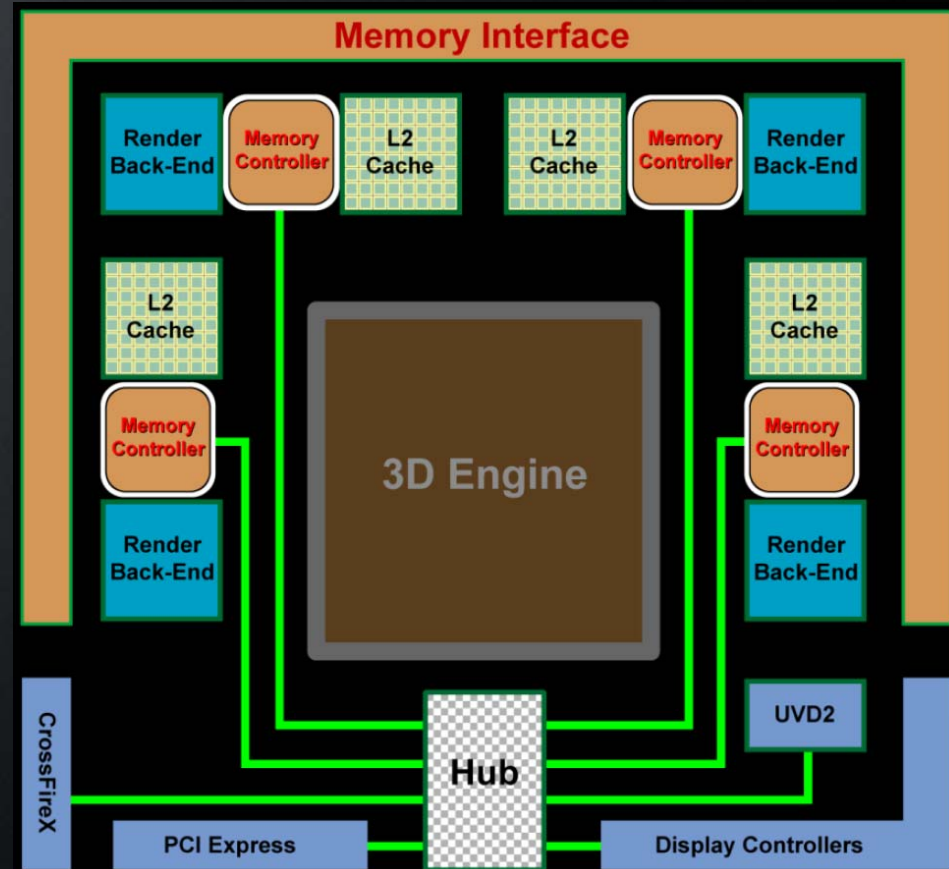
Edge Detect Custom Filter AA

- Enhanced edge-detect filter delivers 12x & 24x CFAA modes
- Avoids blurring by taking additional samples along edges, not across them
- Same memory footprint as 4x & 8x MSAA
- Works with Adaptive AA



Memory Controller Architecture

- New distributed design with hub
- Controllers distributed around periphery of chip, adjacent to primary bandwidth consumers
- Hub handles relatively low bandwidth traffic
 - PCI Express, ATI CrossFireX™ interconnect, UVD2, display controllers, intercommunication



AMD Stream Computing



Stream Software Development Kit

High-level Development Tools

Brook+

- High-level language, C extensions for the GPU
- Based on Brook from Stanford; AMD enhancements will be open-sourced

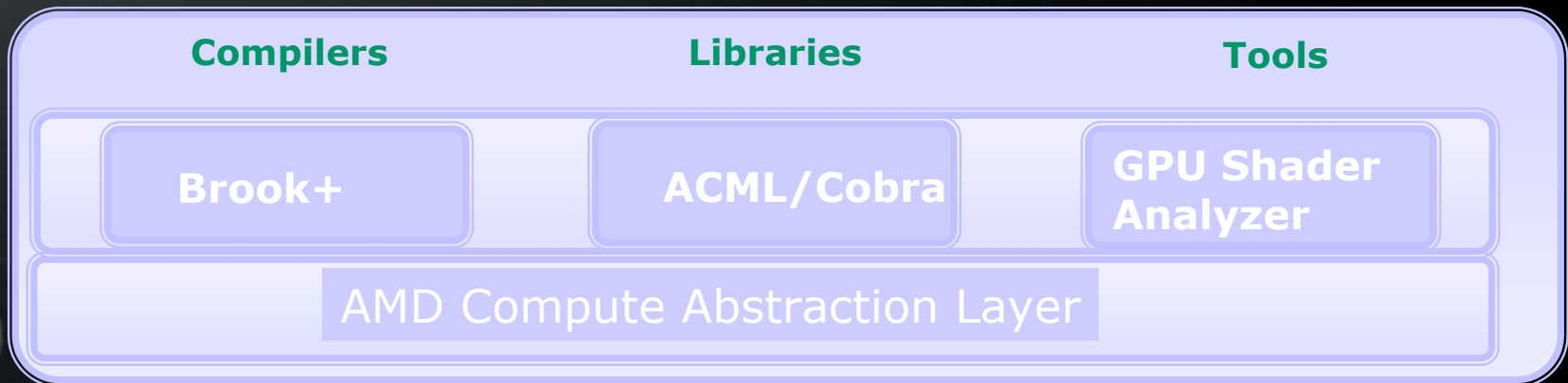
Libraries

- AMD's math library ACML provides GPU-accelerated math functions

Tools

- GPU Shader Analyzer
- AMD Code Analyst

- AMD Compute Abstraction Layer



GPU ShaderAnalyzer

GPU ShaderAnalyzer - MotionBlur10.fx - DX HLSL

File Edit Help

Source Code

Function: PSSceneMain

```
214 clipBiTangent = mul( clipBiTangent, (float3x3)m
215 clipBiTangent = normalize( mul( clipBiTangent,
216 float3 clipTangent = mul( Input.Tan, (float3x3):
217 clipTangent = normalize( mul( clipTangent, (flo
218
219 // Find the projection of our motion into our t
220 Output.Aniso.y = max( 0.0001, abs( g_fTextureSm
221 Output.Aniso.x = max( 0.0001, abs( g_fTextureSm
222
223 return Output;
224 }
225
226 float4 PSSceneMain( VSSceneOut Input ) : SV_TARGET
227 {
228 float2 ddx = Input.Aniso;
229 float2 ddy = Input.Aniso;
230
231 float4 diff = g_txDiffuse.SampleGrad( g_samLine
232 diff.a = 1;
233 return diff*Input.Color;
234 }
```

Compile

HLSL Compiler

Target: ps_4_0

Avoid Flow Control Prefer Flow Control
 Skip Optimization Use DX9 Semantics

Macro Definitions

Symbol	Value
Right-click to add macros.	

Bool Constants

Object Code

Format: Radeon HD 2900 (R600) Assembly

```
; ----- PS Disassembly -----
00 ALU: ADDR(32) CNT(2)
   0 x: MOV R2.x, 0.0f
   1 y: MOV R2.y, 0.0f
01 TEX: ADDR(48) CNT(1)
   1 RESINFO_TEX R2.xy_, R2.xy0x, t
02 ALU: ADDR(34) CNT(8)
   2 t: INT_TO_FLT R122.y, R2.x
   3 w: MUL_IEEE R123.w, R1.z, PS
   4 t: INT_TO_FLT R122.x, R2.y
   5 y: MUL_IEEE R127.y, PV(3).w,
   6 z: MUL_IEEE R123.z, R1.w, PS
   7 x: MUL_IEEE R123.x, PV(4).z,
   8 w: ADD R123.w, R127.y, PV(5)
   9 t: LOG_IEEE/2 R1.w, PV(6).w
03 TEX: ADDR(50) CNT(1) VALID_PIX
   8 SAMPLE_L R1.xyz_, R1.xy0w, t0,
04 ALU: ADDR(42) CNT(3)
   9 x: MUL_IEEE R0.x, R0.x, R1.x
   0 y: MUL_IEEE R0.y, R0.y, R1.y
   1 z: MUL_IEEE R0.z, R0.z, R1.z
```

Compiler Statistics (Using Catalyst 7.12)

Name	GPR	Min	Max	Avg	Est Cycles(Bi)	ALU:TEX(Bi)	Est Cycles(Tri)	ALU:TEX(Tri)	Est Cycles(Aniso)	ALU:TEX(Aniso)	BottleNeck(Bi)	BottleNeck(Tri)	Bot
Radeon HD 2900	4	2.00	2.80	2.27	2.00	1.00	2.40	0.83	2.80	0.71	ALU	TEX	
Radeon HD 2400	4	4.00	4.00	4.00	4.00	2.00	4.00	1.67	4.00	1.43	ALU	ALU	
Radeon HD 2600	4	2.67	2.80	2.67	2.67	1.33	2.67	1.11	2.80	0.95	ALU	ALU	
Radeon HD 3870	4	2.00	2.80	2.27	2.00	1.00	2.40	0.83	2.80	0.71	ALU	TEX	

D3D Assembly Statistics

Shader Version = 4.0
ConstantBuffers = 0, BoundResources = 2, InputParameters = 4, OutputParameters = 1

InstructionCount = 4, TempRegisterCount = 1, TempArrayCount = 0, DefCount = 0, DdCount = 4

AMD Stream Computing

- Documentation
- Developer Forum
- A clear path to OpenCL and DirectX® 11
- Continued support for Brook+/CAL/IL



Next Generation GPUs



Direct3D 11

- Tessellation
 - Hull Shader
 - Domain Shader
 - Tessellator
- Compute Shader
 - Compute Shader on DirectX® 10
 - Integrated with Direct3D
 - Enables broad installed base
- DirectX® 11 on Windows Vista®



OpenCL

- Expecting something to play with in Q1 2009
- Approachable language for accessing heterogeneous computational resources
- Supports parallel execution on single or multiple processors
 - GPU, CPU, GPU + CPU or multiple GPUs
- Based on a subset of ISO C99 with extensions
- For more information see Aaftab Munshi's OpenCL slides in 'Beyond Programmable Shading' course at SIGGRAPH2008



GPU research

- Compute
 - Game Physics/AI
 - Many challenges in Architecture and Software
 - Heterogeneous Computing/Accelerated Computing, CPU + GPU
 - Software layers



Conclusion

- ATI Radeon™ HD 4800 series
 - Teraflop processing power
 - High performance/\$
- Brook+/CAL for compute programming
- Direct3D 11, OpenCL



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