LUNDS UNIVERSITET | LTH LUNDS TEKNISKA HÖGSKOLA

Institutionen för datavetenskap
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Tentamen i kursen
EDAN15: Konstruktion av inbyggda system
(Design of Embedded Systems)

2019-06-03, kl. 14-19

Sal:
MA 9D, 9E, 9F (E:3315)

Hjälpmedel:
Inga

Resultat anslås:
Senast 2019-06-20

Poänggränser:
Max 40 p., för godkännande krävs ca 20 p.

Jourhavande lärare:
Krzysztof Kuchcinski, tel. 22 23414

The answers to the questions can be written in Swedish or English.

Good luck!
Lycka till!

1 (3 p.)

Discuss and give motivations why implementation of embedded systems using a single processor that implements all functionality in software is often not possible or difficult. Compare this solution to a design that has a processor and specialized hardware connected to it. In your discussion evaluate which architecture is better in respect to the following parameters: performance, cost, power consumption and possibility for future upgrades.

2 (3 p.)

Describe informally what are execution rules for data-flow network built of actors. Explain a notion of *actors*, *tokens* and *firing rules*. Use the following two actors to illustrate these notions:

a) an actor that implements addition of two numbers, and
b) a select actor that depending on the control input value (`true` or `false`) selects a token from input `T` for `true` and input `F` for `false`. When selecting one of the inputs (`T` or `F`), the other input has to be neglected, i.e. not selected by a next control token.

Define firings rules for these actors.

3 (3 p.)

The handshaking protocol specifies how data are communicated between Master and Slave units. The protocol has the following phases.

1. Master asserts signal `req` to receive data,
2. Slave puts data on bus and asserts signal `ack`,
3. Master receives data and deasserts signal `req`, and
4. Slave is ready for next request.

Formalize this specifications using Petri nets and prove, using for example reachability trees or graphs, that the master after sending request (`req`) will get data.

Extend the example with two slaves. Draw the new Petri net for this example (you do not need to prove this case).

4 (5 p.)

Write behavioral synthesizable VHDL code that implements a simple ALU unit. The code should include entity declaration and architectural body. The ALU has two 16-bit input `IN1` and `IN2`, a 2-bit control input `sel` which selects one of four operations. It has also one 16-bit output `ALU_OUT`. The following four operations need to be implemented.

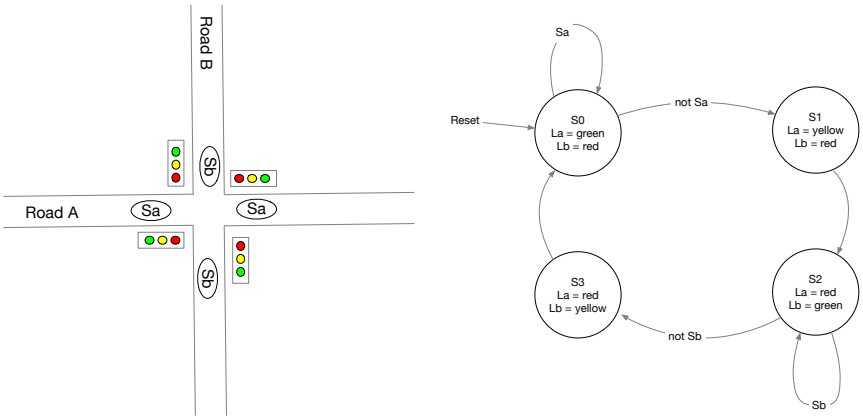
- `AND`– logical bitwise AND operation on inputs `IN1` and `IN2`; output `ALU_OUT = IN1 AND IN2`,
- `OR`– logical bitwise OR operation on inputs `IN1` and `IN2`; output `ALU_OUT = IN1 OR IN2`,
- `add`– add contents of inputs `IN1` and `IN2`; output `ALU_OUT = IN1 + IN2`,

- `sub`– subtract contents of inputs `IN1` and `IN2`; output `ALU_OUT = IN1 - IN2`.

Overflow for `add` and `sub` operations is not signalled.

5 (6 p.)

Write the synthesizeable behavioral VHDL code that implements the traffic light controller for the crossing of roads `A` and `B` depicted in Figure 1.a. The FSM reacts to signals from sensors `Sa` and `Sb` that indicate presence of cars on road `A` ands `B` respectively. The FSM is activated in intervals of 5 seconds. The transitions are active when the signal assigned to them is true. If transition is not marked with any signal it is always active.



a) road crossing b) FSM for traffic light controller

Figure 1: Roads with traffic lights and related FSM.

6 (4 p.)

Assume that the weighted graph depicted in Figure 2 represents tasks and their intercommunications. The weight of an edge represents the communication "cost". Define the appropriate closeness function and find clusters that minimize communication cost. Present consecutive steps of the hierarchical clustering algorithm.

Give the value of your closeness function between the following two clusters for these three cases.

1. {3} and {5},
2. {3} and {6},
3. {5, 7, 8} and {3}.

Which of these three cases is the best to select for clustering in the next step of clustering algorithm, according to your closeness function?

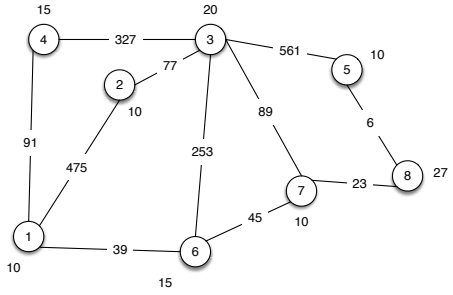


Figure 2: An example system represented as a graph.

7 (5 p.)

Using list scheduling, make the schedule for the data dependency graph depicted in Figure 3. Assume that you can use two adders and two pipelined multipliers. Adders have 1 clock cycle delay and multipliers 2 clock cycles delay (two pipeline stages, 1 cycle for each pipeline stage). Answer the following questions:

a) How do you compute the priorities? Write down the priority for each operation.

b) What is the number of clock cycles for execution of this model?

Give the sequence of steps taken by the list scheduling algorithm that lead to your solution. For each step specify the list of nodes that were considered for scheduling.

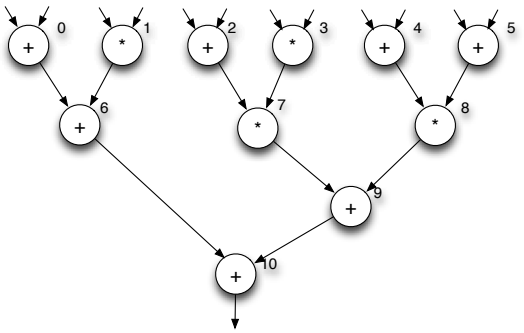


Figure 3: An example of data dependency graph

8 (5 p.)

Describe briefly Rate Monotonic Scheduling (RMS). The presentations should include the following parts:

a) describe the task model and execution assumptions,

b) the method to assign priorities to tasks, and
c) discussion whether RMS can provide the optimal schedule and the condition for scheduliability of tasks.

Draw the RMS schedule for the task set from Table 1 for the first 12 times units.

Task	Period	WCET
1	4	1
2	6	2
3	12	4

Table 1: Task set for RMS scheduling.

9 (3 p.)

What is the formula for power consumption in CMOS technology? Discuss how the power consumption of a design can be minimized considering the parameters of this formula. Specifically, explain how parallelization of computations can be used, not only to speed-up a design, but also to reduce its power consumption.

10 (3 p.)

Discuss briefly the main idea of BIST testability improvement method. In your discussion explain the following parts of BIST:

a) pattern generator,
b) signature analyzer, and
c) BIST controller.

What is the testing procedure and how do you decide whether the unit under test is correct or not. What are advantages and drawbacks of this method?