



LUNDS UNIVERSITET

Lunds Tekniska Högskola

Institutionen för datavetenskap

Krzysztof Kuchcinski

Tentamen i kursen
EDAN15: Konstruktion av inbyggda system
(Design of Embedded Systems)

2018-06-01, kl. 8-13

Sal:

Vic: 2C, 2D (E:1144)

Hjälpmedel:

Inga

Resultat anslås:

Senast 2018-06-20

Poänggränser:

Max 40 p., för godkännande krävs ca 20 p.

Jourhavande lärare:

Krzysztof Kuchcinski, tel. 22 23414

The answers to the questions can be written in Swedish or English.

Good luck!

Lycka till!

1 (3 p.)

Give a short definition of embedded systems. What are the basic parameters considered in the design process? Give at least three most important parameters. Based on these parameters identify specific design challenges and trade-offs for such systems.

2 (3 p.)

Draw a data-flow graph that implements the following computation that has three inputs in_1 , in_2 and in_3 , and one output out .

```
x = in1 + in2
y = x + 1
if (in3 > 11 )
    out = x
else
    out = y
```

In your model, use the following actors.

- actors implementing simple addition of two numbers ($a + b$),
- greater than zero (> 0); producing output *true* or *false* depending on the input value being > 0 or ≤ 0 respectively,
- selector; selecting $input_1$ or $input_2$ depending on *sel* input being *true* or *false*.

3 (3 p.)

Model, using Petri nets, an asynchronous processor control unit with the following characteristics.

- The processor has two registers R0, R1 and two functional units A and B,
- Ready to execute instructions are in buffer I,
- Instructions are issued to be executed when the registers and the functional units they need are available (not used by other instructions),
- there are two types of instructions
 - instruction type 1 requires registers R0 and R1 and functional unit A to execute, and
 - instruction type 2 requires register R1 and functional units A and B to execute.

For drawing your solution start from the partial Petri net structure depicted in Figure 1. Add back edges, if needed.

4 (5 p.)

You are to implement a 2 tap IIR filter in VHDL. The function of the IIR filter is $Y_n = X_n + \frac{1}{2}Y_{n-1} + \frac{1}{4}Y_{n-2}$. X is the input, and Y is the output. Index n denotes the clock cycle n . The VHDL entity for the component is shown in listing 1. You do not need to handle overflow, i.e. you can assume that the

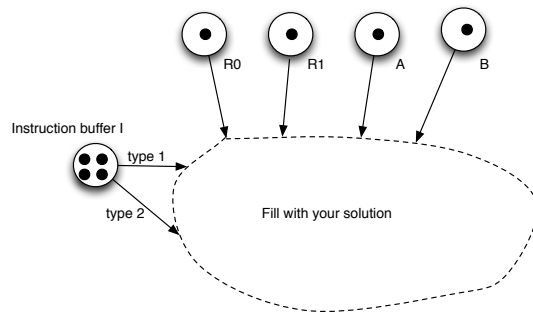


Figure 1: Partial Petri net structure for assignment 3.

output will always fits in 32 bits. *reset* is active high. At a reset the output and the internal state must be set to 0 (Y_n, Y_{n-1} , and Y_{n-2} in the formula). Your implementation must be written in synthesizable behavioral VHDL code.

Listing 1: Write the behavior of for the IIR entity

```
entity IIR is
port (
  clk : in STD_LOGIC;
  reset : in STD_LOGIC;
  X : in STD_LOGIC_VECTOR(0 to 31);
  Y : out STD_LOGIC_VECTOR(0 to 31);
);
end IIR;
```

5 (6 p.)

Figure 2 depicts a diagram for a Mealy state machine. Write the VHDL code for the entity and architecture that implements this machine. Assume that at signal *reset* = '0' the machine should be initiated to state S0.

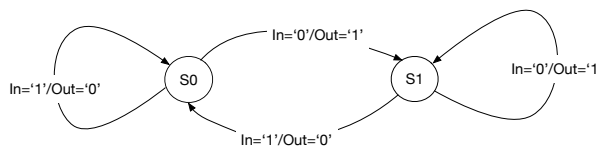


Figure 2: Specification of the state machine.

6 (4 p.)

Assume that the weighted graph depicted in Figure 3 represents tasks and their intercommunications. The weight of an edge represents the communication

“cost”. Define the appropriate closeness function and find clusters that minimize communication cost. Present consecutive steps of the hierarchical clustering algorithm.

Give the value of your closeness function between the following two clusters for these three cases.

1. $\{P3\}$ and $\{P5\}$,
2. $\{P3\}$ and $\{P6\}$,
3. $\{P6, P7\}$ and $\{P8\}$.

Which of these three cases is the best to select for clustering in the next step of clustering algorithm, according to your closeness function?

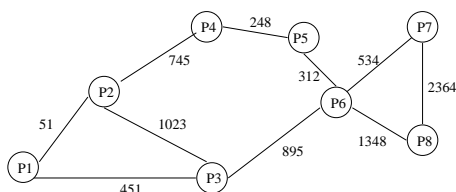


Figure 3: An example system represented as a graph.

7 (5 p.)

Using list scheduling, make the schedule for the data dependency graph depicted in Figure 4. Assume that you can use two adders and two pipelined multipliers. Adders have 1 clock cycle delay and multipliers 2 clock cycles delay (two pipeline stages, 1 cycle for each pipeline stage). Answer the following questions:

- a) How do you compute the priorities? Write down the priority for each operation.
- b) What is the number of clock cycles for execution of this model?

Give the sequence of steps taken by the list scheduling algorithm that lead to your solution. For each step specify the list of nodes that were considered for scheduling.

8 (5 p.)

Describe briefly Rate Monotonic Scheduling (RMS). The presentations should include the following parts:

- a) describe the task model and execution assumptions,
- b) the method to assign priorities to tasks, and
- c) discussion whether RMS can provide the optimal schedule and the condition for schedulability of tasks.

Draw the RMS schedule for the task set from Table 1 for the first 12 times units.

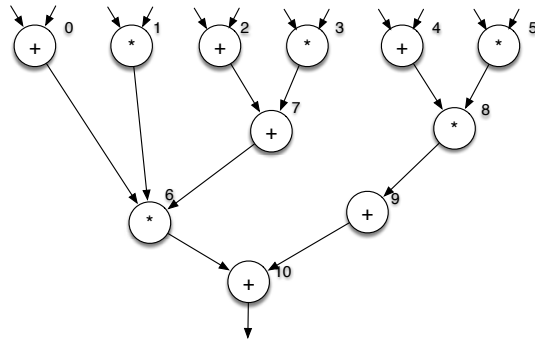


Figure 4: An example of data dependency graph

Task	Period	WCET
1	3	1
2	6	2
3	12	3

Table 1: Task set for RMS scheduling.

9 (3 p.)

What is the formula for power consumption in CMOS technology? Discuss how the power consumption of a design can be minimized considering the parameters of this formula. Specifically, explain how parallelization of computations can be used, not only to speed-up a design, but also to reduce its power consumption.

10 (3 p.)

Discuss briefly the SCAN path testability improvement technique. In the discussion include the following points:

- a) the general idea of the SCAN path, and
- b) give the motivation why SCAN path improves test generation and testing time.