Lunds universitet
Lunds Tekniska Högskola

Institutionen för datavetenskap
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Tentamen i kursen
EDAN15: Konstruktion av inbyggda system
(Design of Embedded Systems)

2014-06-02, kl. 8-13

Sal:
Sparta: A-B

Hjälpmedel:
Inga

Resultat anslås:
Senast 2014-06-19

Poänggränser:
Max 40 p., för godkännande krävs ca 20 p.

Jourhavande lärare:
Krzysztof Kuchcinski, tel. 22 23414

The answers to the questions can be written in Swedish or English.

Good luck!
Lycka till!

1 (3 p.)

Give a short definition of embedded systems. What are basic characteristics of embedded systems? Based on these characteristics identify specific design challenges for such systems.

2 (2 p.)

Based on the VHDL code given below complete the following table with right signal values. The waveform for signal a is given in the table.

```vhdl
architecture rtl of example is
begin
  b <= a;
  c <= b after 10ns;
end
```

	0 ns	10 ns	10 ns + δ	10 ns + 2δ	...	20 ns	20 ns + δ	20 ns + 2δ	...
a	0	1	1	1	1	0	0	0	0
b	0								
c	0								

3 (3 p.)

Model, using Petri nets, an asynchronous processor control unit with the following characteristics.

- The processor has two registers R0, R1 and two functional units A and B,
- Ready to execute instructions are in buffer I,
- Instructions are issued to be executed when the registers and the functional units needed by them are available (not used by other instructions),
- there are two types of instructions to execute
    - instruction type 1 requires register R1 and functional unit A to execute, and
    - instruction type 2 requires registers R0, R1 and functional unit B to execute.

4 (6 p.)

Write the behavioral VHDL code for the entity and architecture that implements a simple *sequence detector*. The detector has clock, x_in, y_in inputs and z_out output of type std_logic. On each rising edge of the clock signal the sequence detector checks the value on x_in. Once it has detected a sequence of 110 on the x_in input it generates an output equal to the negation of the y_in input. If the sequence was not detected, it outputs the value of y_in. The output of the circuit is on the z_out line.

5 (6 p.)

Write the synthesizeable behavioral VHDL code for a process which implements a simple ALU unit. The ALU has a 2-bit control input which selects one of four operations, +, -, bitwise and operation and bitwise or operation between two 16-bit inputs. Assume combinatorial implementation of ALU.

6 (4 p.)

Assume that the application graph, specified as a weighted graph, depicted in Figure 1 represents the tasks and their intercommunications for a certain application. The weight of an edge represents the communication "cost" while the weight of a node is the "size" of the task in a partition. Assuming that we want to use a clustering algorithm which will group together tasks, give an expression which defines a closeness function for such an algorithm. The closeness function has to make it possible to minimize the communication cost between partitions.

Give the value of your closeness function between the following two clusters for these three cases.

1. {1} and {2},
2. {1} and {4},
3. {3, 7} and {5, 8}.

Which of these three cases is the best to select for clustering in the next step of clustering algorithm according to your closeness function?

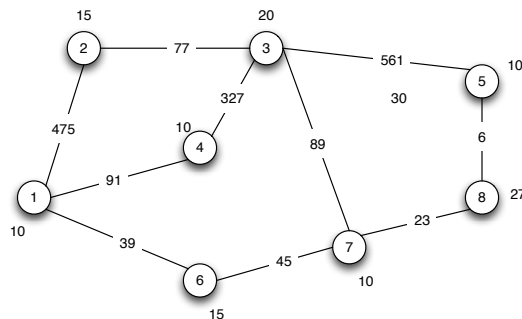Make the hierarchical clustering of this graph using your closeness function.

Figure 1: An example of an application graph for assignment 6.

7 (5 p.)

Using list scheduling, make the schedule for the data dependency graph depicted in Figure 2. Assume that you can use two adders and two pipelined multipliers. Adders have 1 clock cycle delay and multipliers 2 clock cycles delay (two pipeline stages, 1 cycle for each pipeline stage). Answer the following questions:

a) How do you compute the priorities? Write down the priority for each operation.
b) What is the number of clock cycles for execution of this model?

Give the sequence of steps that lead to your solution. For each step give the list of nodes that were considered for scheduling.

8 (5 p.)

Describe briefly Rate Monotonic Scheduling (RMS). The description should include the following parts:

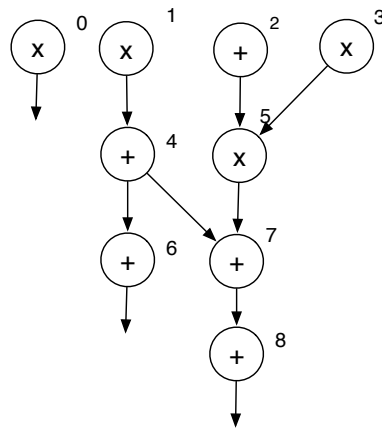a) what are parameters and assumptions for tasks that RMS uses,

Figure 2: An example of data dependency graph

b) the method to assign priorities, and

c) discussion whether RMS can provide optimal schedule and the condition for schedu-
   liability of tasks. What does optimality mean for RMS?

Draw the RMS schedule for the task set from Table 1.

Task	Period	WCET
1	6	1
2	8	3
3	12	2

Table 1: Task set for RMS scheduling.

9 (3 p.)

What is the formula for power consumption in CMOS technology? Discuss how the
power consumption of a design can be minimized. Specifically, explain how parallelization
of computations can be used, not only to speed-up a design, but also to reduce its power
consumption. Support your discussion with reference to the power consumption formula.

10 (3 p.)

Discuss briefly the main idea of BIST testability improvement method. In your discussion
explain the following parts of BIST:

a) pattern generator,

b) signature analyzer, and

c) BIST controller.

What is the testing procedure and how do you decide whether the unit under test is correct
or not. What are advantages and drawbacks of this method?