Institutionen för datavetenskap
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Tentamen i kursen
EDAN15: Konstruktion av inbyggda system
(Design of Embedded Systems)

2013-06-03, kl. 8-13

Sal:
Vic:3C-D

Hjälpmedel:
Inga

Resultat anslås:
Senast 2013-06-17

Poänggränser:
Max 40 p., för godkännande krävs ca 20 p.

Jourhavande lärare:
Krzysztof Kuchcinski, tel. 22 23414

The answers to the questions can be written in Swedish or English.

Good luck!
Lycka till!

1 (3 p.)

Explain the term "design space exploration". What does it mean for embedded systems design? What are the typical design parameters considered during design space exploration? Use an example of a cell phone to discuss typical parameters that need to be considered during exploration.

2 (3 p.)

VHDL simulator is implemented as an *event-driven* simulator. Describe briefly the main idea of event-driven simulation. What is an event and how is time progress handled in this simulation paradigm?

3 (3 p.)

Draw the data-flow graph for the following code assuming that each actor may contain at most one arithmetic operation.

```
x <= a + b;
case x is
  when 0 => y <= a + 1;
  when 1 => y <= a - 1;
  when 2 => y <= 2 * a;
  when others => y <= b;
end case;
```

Specify the firing rules and functions for each actor in your model. A function specifies an actor output as a function of its inputs, i.e., $out = f(inputs)$.

4 (5 p.)

Write the synthesizeable behavioral VHDL code that implements the synchronous finite state machine (FSM) depicted in figure 1. This FSM detects pattern 110 and it has initial state S_0. Implement this FSM with *asynchronous* reset and assume active low reset. The reset signal forces the FSM to return to state S_0.

The arcs of the FSM are labeled with two binary values separated by "/" indicating input and output signal respectively, e.g. 0/1 indicates input signal equal 0 and output signal equal 1.
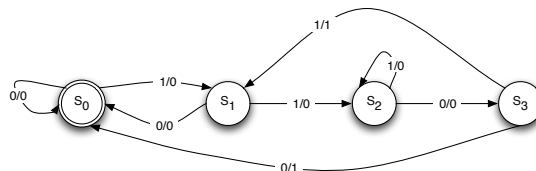

Figure 1: FSM model for an elevator controller.

5 (6 p.)

Write the synthesizeable behavioral VHDL code that implements the following C function. The computation should be done using 32 bit integers and it should take several clock cycles. You can assume that the inputs are available when needed on ports a and b. The output is sent to port r.

```c
int foo(int a, int b) {
  int result = 0;
  while (b>0) {
    result += a;
    b--;
  }
  return result;
}
```

6 (4 p.)

Assume that the application graph, specified as a weighted graph, depicted in Figure 2 represents the tasks and their intercommunications for a certain application. The weight of an edge represents the communication "cost" while the weight of a node is the "size" of the task in a partition. Assuming that we want to use a clustering algorithm which will group together tasks, give an expression which defines a closeness function for such an algorithm. The closeness function has to make it possible to minimize the communication cost between partitions.

Give the value of your closeness function between the following two clusters for these three cases.

1. {1} and {2},
2. {1} and {3},
3. {3, 5} and {7, 8}.

Which of these three cases is the best to select for clustering in the next step of clustering algorithm according to your closeness function?

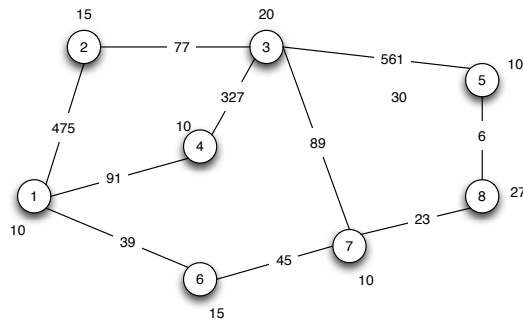Make the hierarchical clustering of this graph using your closeness function.

Figure 2: An example of an application graph for assignment 6.

7 (5 p.)

Using list scheduling, make the schedule for the data dependency graph depicted in Figure 3. Assume that you can use two adders and two pipelined multipliers. Adders have 1 clock cycle delay and multipliers 2 clock cycles delay (two pipeline stages, 1 cycle for each pipeline stage). Answer the following questions:

    a) How do you compute the priorities? Write down the priority for each operation.

    b) What is the number of clock cycles for execution of this model?

Give the sequence of steps that lead to your solution. For each step give the list of nodes that were considered for scheduling.
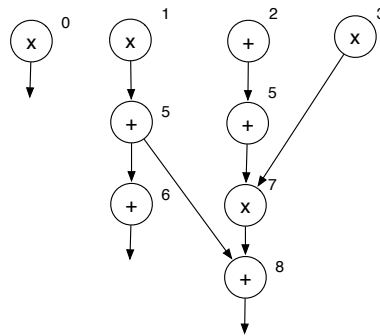

Figure 3: An example of data dependency graph

8 (5 p.)

Describe briefly Earliest Deadline First (EDF) scheduling. The description should include the following parts:

    a) necessary assumptions about each task and its parameters,

    b) the method to assign priorities, and

    c) discussion whether EDF can provide optimal schedule and the condition for schedulability of tasks. What does optimality mean for RMS?

  Draw the EDF schedule for the task set from Table 1.

Task	Period	WCET
1	6	1
2	8	3
3	12	5

Table 1: Task set for EDF scheduling.

9 (3 p.)

What is the formula for power consumption in CMOS technology? Discuss how the power consumption of a design can be minimized. Specifically, explain how parallelization of computations can be used, not only to speed-up a design, but also to reduce its power consumption. Support your discussion with reference to the power consumption formula.

10 (3 p.)

Discuss briefly the SCAN path testability improvement technique. In the discussion include the following points:

   a) the general idea of the SCAN path, and
   b) why SCAN path improves test generation and testing time.