LUNDS TEKNISKA HÖGSKOLA
Lunds universitet

Institutionen för datavetenskap
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Tentamen i kursen
EDA380: Konstruktion av inbyggda system
(Design of Embedded Systems)

2006-05-29, kl. 14-18

Sal:
MA 10A-C

Hjälpmedel:
Inga

Resultat anslås:
Senast 2006-06-12

Poänggränser:
Max 40 p., för godkännande krävs ca 20 p.

Jourhavande lärare:
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The answers to the questions can be written in Swedish or English.

Lycka till!

1 (3 p.)

During development of an embedded system a designer need to consider different kind of implementation trade-offs. Typically one need to consider different implementation options and their effect on the final design parameters, such as performance, cost and power consumption. Discuss typical design trade-offs and their effect on the final design.

2 (6 p.)

Figure 1 depicts a diagram for a Mealy state machine. Write the VHDL code for the entity and architecture which implements this machine. Assume that at signal `reset = '0'` the machine should be initiated to state `S0`.

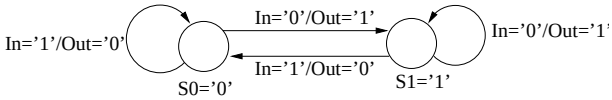

Figure 1: Specification of the state machine.

3 (4 p.)

Figure 2 depicts a Petri net that has two parallel tasks (task 1 contains P_1, P_2 and P_3 and task 2 P_4, P_5 and P_6) that have access to critical sections *CR1* and *CR2*. The initial marking of this net has one token in P_1 and one token in P_4. Only one task at a time can be in the critical section. Complement this Petri net with additional part that models exclusive access to critical sections *CR1* and *CR2*, that is only one critical section can have a token in any possible markings of this net.

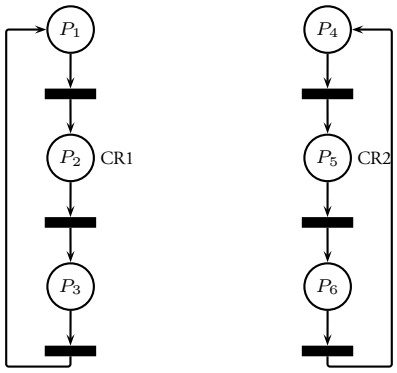

Figure 2: The Petri net with two critical sections *CR1* and *CR2*

4 (3 p.)

FIR (Finite Impulse Response) filters are one of the most basic building blocks used in digital signal processing. The output y of an N-tap FIR filter is given by the equation

below

$$y_t = a_0 x_t + a_1 y_{t-1} + \cdots + a_N y_{t-N-1}$$

where *x* is the input to the filter and $a_0, a_1, \ldots, a_{N-1}$ are the filter's coefficients.

Draw the data-flow graph for the 4-tap FIR filter.

5 (6 p.)

Write synthesizeable VHDL code for the entity and architecture that implements the 4-tap FIR filter presented in the assignment above. Assume that the filter's coefficients are integers and are equal $a_0 = 2$, $a_1 = 5$, $a_2 = 4$ and $a_3 = 3$. In your design try to avoid multipliers to perform multiplication by a constant.

6 (4 p.)

Assume that the weighted graph, such as depicted in Figure 3, represents tasks and their intercommunications. The weight of an edge represents the communication "cost" while the weight of a node is the "size" of the task in a partition. Assuming that we want to use a clustering algorithm which will group together tasks into clusters, give an expression which defines a closeness function for such an algorithm. The closeness function has to make it possible to minimize the communications cost between partitions.

Give the value of your closeness function for the following sets of two nodes

1. T_1 and T_2,
2. T_1 and T_5,
3. T_0 and T_3.

Which of these three cases is the best to select for clustering in the next step of clustering algorithm according to your closeness function?

Make the hierarchical clustering of this graph.

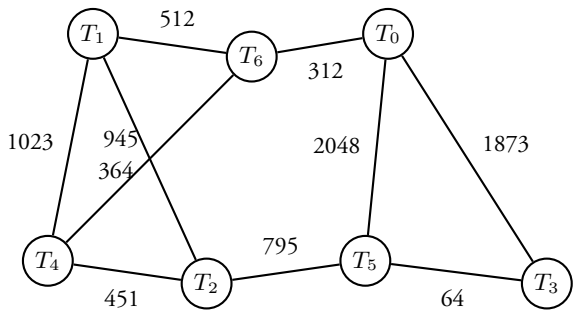

Figure 3: An example of a partitioning graph.

7 (4 p.)

Using list scheduling, make a schedule for a data-flow graph depicted in Figure 4. Assume that you can use one adder and two multipliers. Adders have 1 clock cycle delay and multipliers 2 clock cycles delay. Answer the following questions:

a) What priorities do you use in your list scheduling?
b) What is the number of clock cycles for execution of this model?

Give sequence of steps of the list scheduling algorithm.

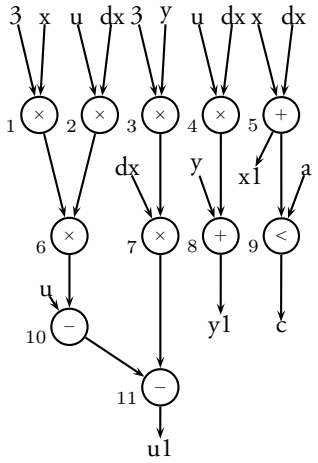

Figure 4: An example of data-flow graph.

8 (3 p.)

Describe briefly Earliest Deadline First (EDF) dynamic priority scheduling. The presentations should include the following parts:

a) necessary assumptions about each task and its parameters,
b) the method to assign priorities, and
c) discussion whether EDF can provide optimal schedule.

9 (3 p.)

What is the formula for power consumption in CMOS technology? Discuss how power consumption of a design can be minimized. Specifically, explain how parallelization of computations can be used not only to speed-up a design but also to reduce power consumption. Support your discussion with reference to the power consumption formula.

10 (4 p.)

Discuss briefly the main idea of SCAN path testability improvement technique. In the discussion include the following points:

a) the general idea of the SCAN path, and
b) why SCAN path improves test generation and testing time.