LUNDS TEKNISKA HÖGSKOLA
Lunds universitet

Institutionen för datavetenskap
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Tentamen i kursen
E380: Konstruktion av inbyggda system
(Design of Embedded Systems)

2005-08-23, kl. 14-19

Sal:
MA8

Hjälpmedel:
Inga

Resultat anslås:
Senast 2005-09-06

Poänggränser:
Max 40 p., för godkännande krävs ca 20 p.

Jourhavande lärare:
Kris Kuchcinski, tel. 22 23414

The answers to the questions can be written in Swedish or English.

Lycka till!

1 (3 p.)

Discuss and give motivations why implementation of embedded systems using a single processor that implements all functionality in software is often not possible or difficult. What are advantages and drawbacks of such a solution? In your discussion address importance of design parameters, such as performance, cost and power consumption.

2 (4 p.)

Explain main ideas behind the following design flow models:

- stepwise refinement model,
- hardware/software co-design,
- top-down model,
- bottom-up model.

3 (3 p.)

Draw simple Petri nets which model a) sequential execution, b) parallel execution, and c) non-deterministic choice.

4 (4 p.)

Describe informally what are execution rules for data-flow network built of actors. Explain a notion of *actors*, *tokens* and *firing rules*. Use the following two actors to illustrate these notions:

a) an actor that implements addition of two numbers, and
b) a select actor that depending on the control input value (`true` or `false`) selects a token from input `T` for `true` and input `F` for `false`.

Define firings rules for these actors.

5 (6 p.)

Write the VHDL code for the entity and architecture that implements a simple *sequence detector*. The detector has `enable`, `x_in`, `y_in` inputs ans `z_out` output of type bit. Once it has been enables, it searches for a sequence of `110` on the `x_in` input. When the `110` sequence is found, it generates an output equal to the negation of the `y_in` input. The output of the circuit is on the `z_out` line.

6 (4 p.)

Assume that the weighted graph, such as depicted in Figure 1, represents tasks and their intercommunications. The weight of an edge represents the communication "cost" while the weight of a node is the "size" of the task in a partition. Assuming that we want to partition the task graph into two partitions, give an expression which defines a cost function for a partitioning algorithm. The cost function has to make it possible to minimize the communications cost while making partitions of a similar size (as much as possible).

How can you control the minimization of communication costs vs. keeping the sizes of partitions similar?

Give the value of your cost function for two different partitionings

1. partition 1: P2, P3, P4, P7, P10 and partition 2: P1, P5, P6, P8, P9
2. partition 1: P2, P4, P7, P9, P10 and partition 2: P1, P3, P5, P6, P8

Which partition of the two specified above is better?

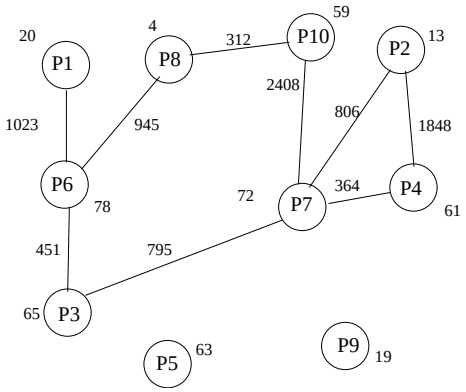

Figure 1: An example system represented as a graph.

7 (4 p.)

Using list scheduling, make a schedule for a data-flow graph depicted in Figure 2. Assume that you can use one adder and two multipliers. Adders have 1 clock cycle delay and multipliers 2 clock cycles delay. Answer the following questions:

a) What priorities do you use in your list scheduling?
b) What is the number of clock cycles for execution of this model?

Give sequence of steps of the list scheduling algorithm.

8 (4 p.)

Describe briefly Earliest Deadline First (EDF) dynamic priority scheduling. The presentations should include the following parts:

a) necessary assumptions about each task and its parameters,
b) the method to assign priorities, and
c) discussion whether EDF can provide optimal schedule.

9 (4 p.)

What is the formula for power consumption in CMOS technology? Discuss how power consumption of a design can be minimized. Specifically, explain how parallelization of computations can be used not only to speed-up a design but also to reduce power consumption. Support your discussion with reference to the power consumption formula.

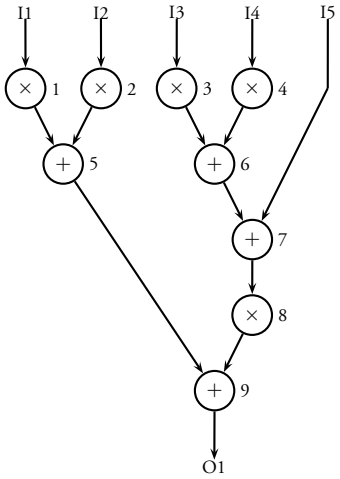

Figure 2: An example of data-flow graph

10 (4 p.)

Discuss briefly the main idea of BIST testability improvement method. In your discussion explain the following parts of BIST:

a) pattern generator,
b) signature analyzer, and
c) BIST controller.

What is the testing procedure and how do you decide whether the unit under test is correct or not. What are advantages and disadvantages of this method?