LUNDS TEKNISKA HÖGSKOLA
Lunds universitet

Institutionen för datavetenskap
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Tentamen i kursen
E380: Konstruktion av inbyggda system
(Design of Embedded Systems)

2005-05-28, kl. 14-19

Sal:
MA8

Hjälpmedel:
Inga

Resultat anslås:
Senast 2005-06-11

Poänggränser:
Max 40 p., för godkännande krävs ca 20 p.

Jourhavande lärare:
Kris Kuchcinski, tel. 22 23414

The answers to the questions can be written in Swedish or English.

Lycka till!

1 (3 p.)

Give a short definition of embedded systems and discuss basic characteristics of such systems. Compare them with workstations and PC computer systems. Point out differences and similarities. Illustrate your discussion with examples of embedded systems.

2 (3 p.)

Discuss a typical design methodology for embedded systems. Where different design activities, such as design specification, design partitioning, component allocation, and communication synthesis are performed?

3 (4 p.)

Write the VHDL code for the entity and architecture that implements a counter. The counter counts from 1 to 3 and has a reset signal. Implement two versions of the counter with *synchronous* and *asynchronous* reset. Assume that at signal `reset = '0'` the counter should be initiated to 0.

4 (4 p.)

Describe informally what are execution rules for data-flow network built of actors. Explain a notion of *actors*, *tokens* and *firing rules*. Use the following two actors to illustrate these notions:

a) an actor that implements addition of two numbers, and
b) a select actor that depending on the control input value (`true` or `false`) selects a token from input `T` for `true` and input `F` for `false`.

Define firings rules for these actors.

5 (4 p.)

The following VHDL processes seems to work when verified in a simulator, but after synthesis the behavior is different on a FPGA. Rewrite the code so it behaves correct after synthesis.

Assume that `OUTPUT`, `A`, `B` and `start` are ports defined in the entity declaration.

```
signal NS, CS : STATE_TYPE;
signal O1, O2 : std_logic_vector(0 to 31);

process (clk, rst)   -- synchronous process
begin
   if clk = '1' then
     CS <= NS;
   end if;
end process;

process (NS) -- combinatorial process
begin
```

```
   case CS is
     when S0 => if start = '1' then
                  NS <= S1;
                  O1 <= foo(A);
                end if;
     when S1 => NS <= S2;
                O2 <= bar(O1, B);
     when S2 => OUTPUT <= bar2(O1, O2);
                NS <= S0;
     when others => NS <= S0;
   end case;
end process;
```

6 (4 p.)

Give the values assigned to signals and variables by the part of the VHDL process included below.

```
P1: process
    variable a, b : integer;
begin
       :
   -- initial values of s1 = 1, s2 = 0, a = 0, b = 0
   s1 <= 10;
   a := s1;
   b := 11;
   s2 <= b + s1;
   -- give values of s1, s2, a, b here (1)
   wait for 10 ns;
   -- give values of s1, s2, a, b here (2)
       :
end process;
```

7 (6 p.)

Using list scheduling, make a schedule for a data-flow graph depicted in Figure 1. Assume that you can use one adder and two multipliers. Adders have 1 clock cycle delay and multipliers 2 clock cycles delay. Answer the following questions:

a) What priorities do you use in your list scheduling?
b) What is the number of clock cycles for execution of this model?

8 (4 p.)

Use the RMS analysis to check sufficient condition for the following task sets schedulability with RMS. Are the tasks schedulable?

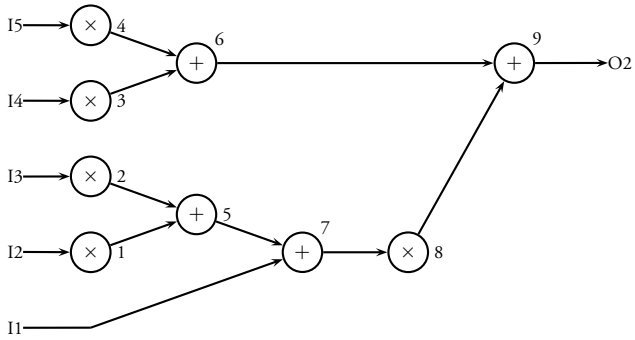

Figure 1: An example of data-flow graph

Task set 1

Task	Period	Worst execution time
1	100	20
2	150	40
3	300	60

Task set 2

Task	Period	Worst execution time
1	3	1
2	5	1
3	6	1
4	10	2

9 (4 p.)

What are the main sources of power consumption in CMOS technology (use an equation for power consumption to support your discussion)? How can power consumption be minimized when designing hardware?

10 (4 p.)

Discuss briefly the main idea of BIST testability improvement method. In your discussion explain the following parts of BIST:

a) pattern generator,
b) signature analyzer, and
c) BIST controller.

What is the testing procedure with this method and what are advantages and disadvantages.