LUNDS TEKNISKA HÖGSKOLA
Lunds universitet

Institutionen för datavetenskap
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Tentamen i kursen
E380: Konstruktion av inbyggda system
(Design of Embedded Systems)

2004-08-23, kl. 14-19

Sal:
MA10E

Hjälpmedel:
Inga

Resultat anslås:
Senast 2004-09-06

Poänggränser:
Max 40 p., för godkännande krävs ca 20 p.

Jourhavande lärare:
Kris Kuchcinski, tel. 22 23414

The answers to the questions can be written in Swedish or English.

Lycka till!

1 (3 p.)

Give a short definition of embedded systems and discuss basic characteristics of such systems. Compare them with workstations and desktop computer systems. Point out differences and similarities. Illustrate your discussion with examples of embedded systems.

2 (3 p.)

VHDL simulator is implemented as an event-driven simulator. Describe briefly the main idea of event-driven simulation. What is an event and how is time handled in this simulation paradigm?

3 (4 p.)

Using data-flow networks model a simple filter which reads in each clock cycle one unsigned integer value form input in and outputs a value equal an average over the last four read values. This means $(in_{-3} + in_{-2} + in_{-1} + in_0)/4$. Explain what actors you use and what are their firing rules.

4 (6 p.)

Write the VHDL code for the entity and architecture that implements a counter. The counter counts from 1 to 3 and has a reset signal. Implement two versions of the counter with *synchronous* and *asynchronous* reset. Assume that at signal `reset = '0'` t the counter should be initiated to 0.

5 (6 p.)

Write the VHDL code that implements a simple filter (the same as specified in question 3) which reads in each clock cycle one 8-bit unsigned integer form input in and outputs a value equal an average over last four read values. This means $(in_{-3} + in_{-2} + in_{-1} + in_0)/4$. In this assignment you can ignore possible overflow during computations.

6 (3 p.)

Draw simple Petri nets which model sequential execution, parallel execution and nondeterministic choice.

7 (4 p.)

Using list scheduling, make a schedule for a data-flow graph depicted in Figure 1. Assume that you can use one adder and one multiplier. Adders have 1 clock cycle delay and multipliers 2 clock cycles delay. Answer the following questions:

a) What priorities do you use in your list scheduling?
b) What is the number of clock cycles for execution of this model?

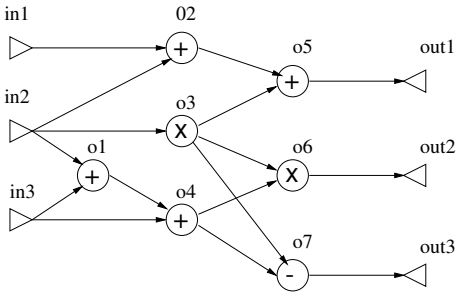

Figure 1: An example of data-flow graph

8 (4 p.)

Describe briefly Earliest Deadline First (EDF) dynamic priority scheduling. The presentations should include the following parts:

a) necessary assumptions about each task and its parameters,
b) the method to assign priorities, and
c) discussion whether EDF can provide optimal schedule.

9 (3 p.)

What is the formula for power consumption in CMOS technology? Discuss how power consumption of a design can be minimized. Specifically, explain how parallelization of computations can be used not only to speed-up a design but also to reduce power consumption. Support your discussion with reference to power consumption formula.

10 (4 p.)

Discuss briefly the main idea of BIST testability improvement technique. In the discussion include the following points:

a) the general idea of the BIST,
b) what changes are needed in the design to include BIST,
c) what are potential problems with this technique, and
d) why BIST makes it possible to perform on-speed testing (i.e., tests at full speed of the circuits).