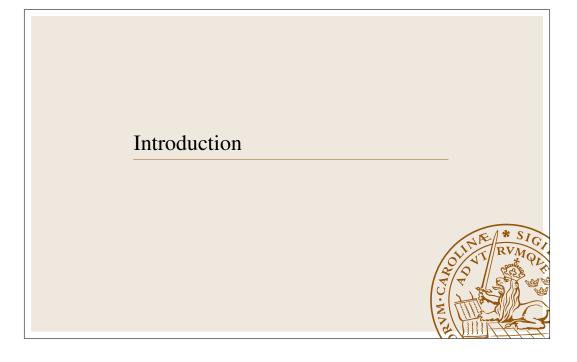
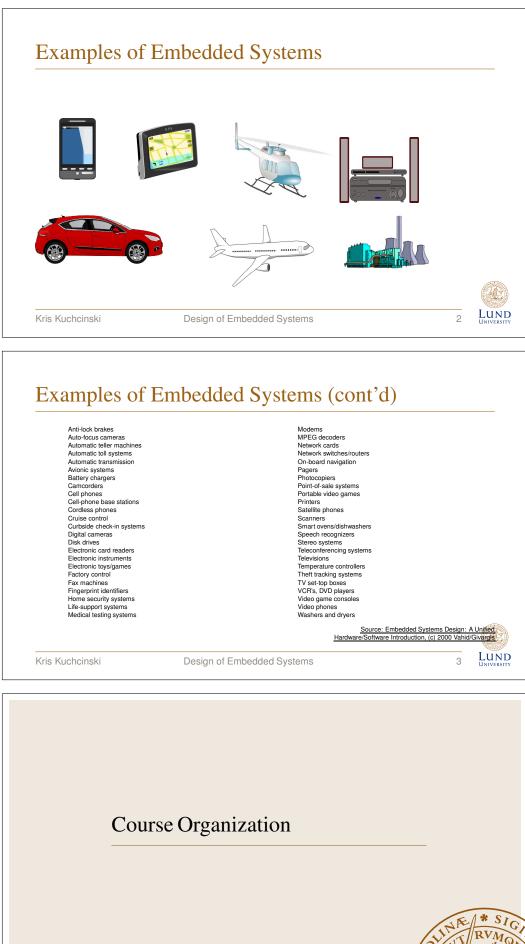
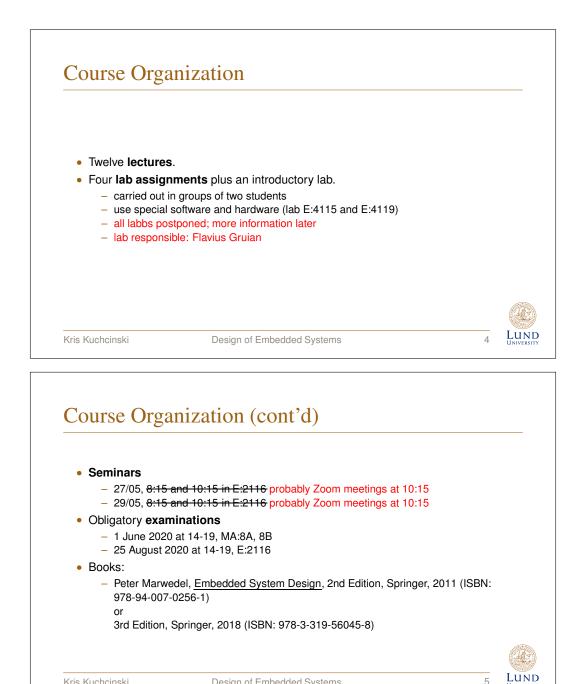


Outline		
Introduction		
Course Organization		
General introduction	, definition of the field	
Embedded Systems	Examples	
Embedded Systems	Design Methodologies	
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Kris Kuchcinski	Design of Embedded Systems	1 Lun





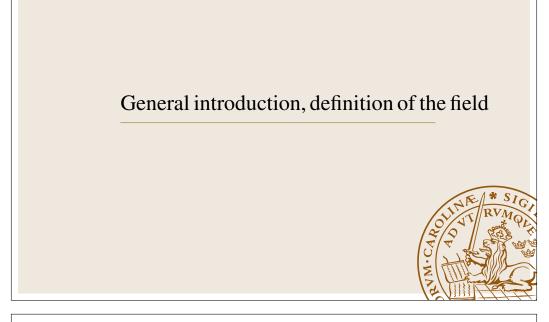


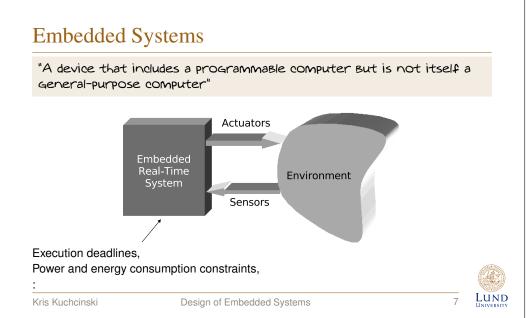


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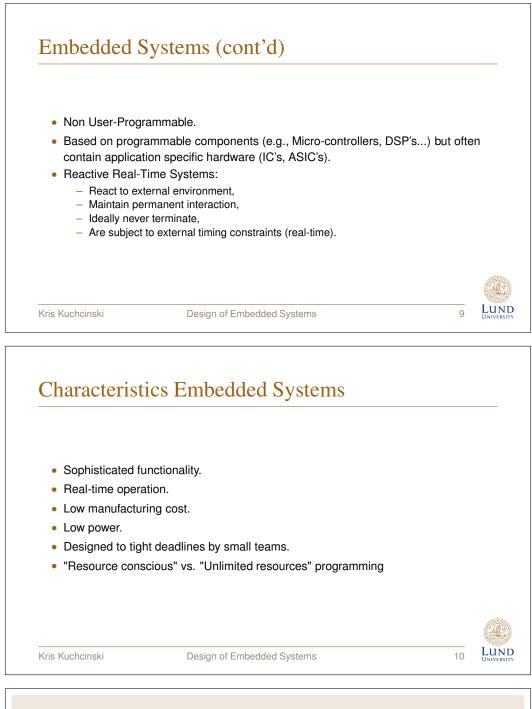
Design of Embedded Systems

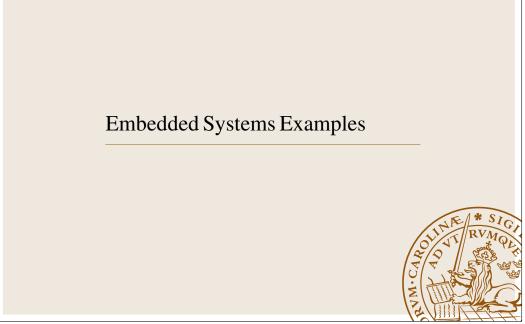
Lectures **Preliminary Schedule** Date Content 20-03-23 Introduction, motivation, etc. 20-03-27 Design methodology (HW/SW co-design, etc) 20-03-30 VHDL introduction 20-04-03 VHDL for synthesis 20-04-06 Computational models 20-04-27 Design representations 20-05-04 System partitioning 20-05-08 Allocation, assignment 20-05-11 and scheduling 20-05-15 Communication synthesis 20-05-18 Testability 20-05-25 Low-power design | ARM presentation LUND Kris Kuchcinski 6 Design of Embedded Systems

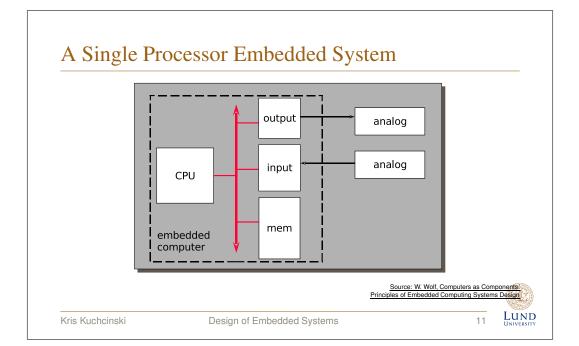


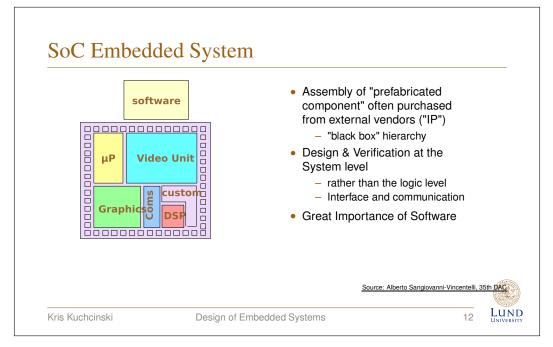


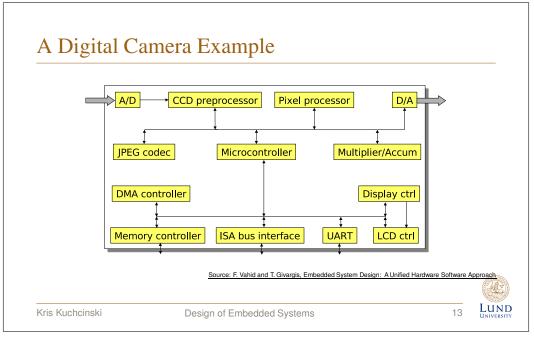
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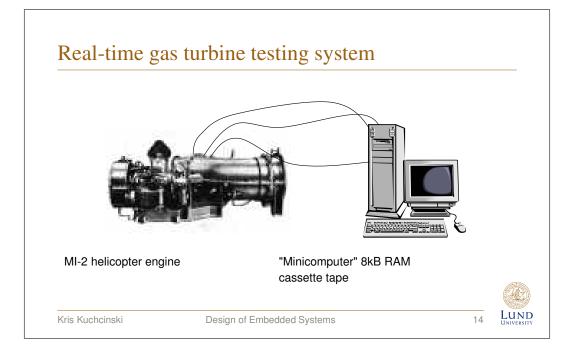


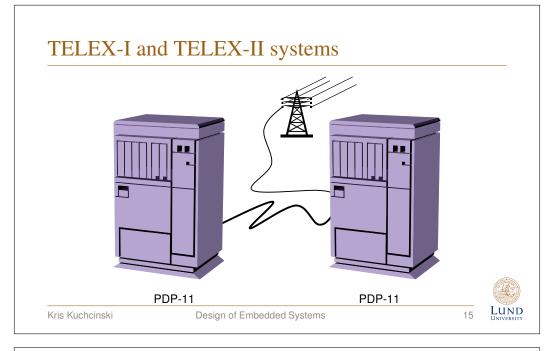






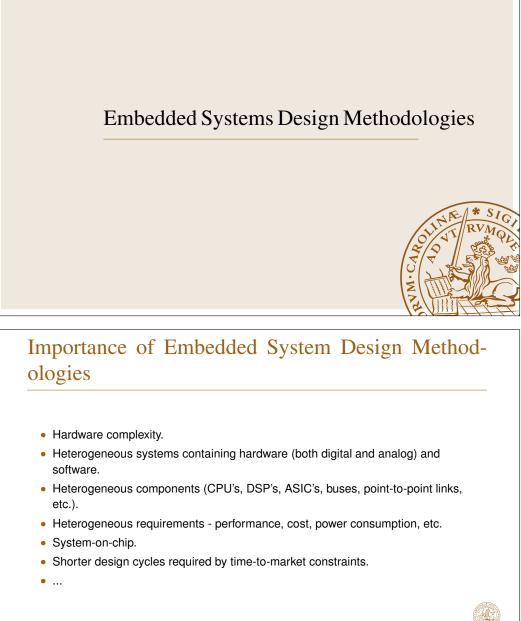








Component class	Implements	Compiler	Specification	
DSP processor	Low data-rate DSP	(Retargetable)	Assembly	
	Slow control loops	code generator	С	
	Appl. Spec. alg.	High level synth.		
Microcontroller	User interface	C compiler	С	
	Slow control loops			
Hardware accelerator	High data-rate DSP	High level synth.	C, VHDL	
	RT level synth.		Verilog	
Communication	Internal & external	Memory mgmt.	Data-sheets	
blocks and	communication	(A)synchronous		
memory	Storage & buffering	interface synth.		
Others	Usually FSMD's	RT level synth.	VHDL	
	<ul> <li>clock generators</li> </ul>	Asynchronous		
	<ul> <li>DMA blocks</li> </ul>	synth.		

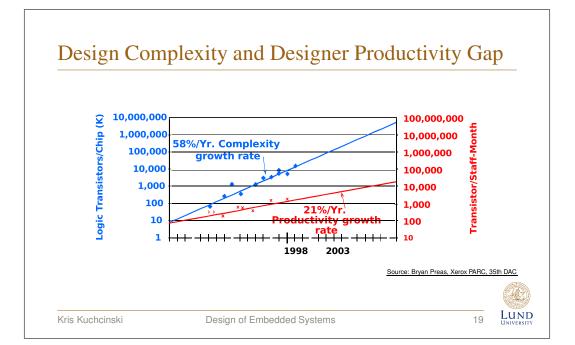


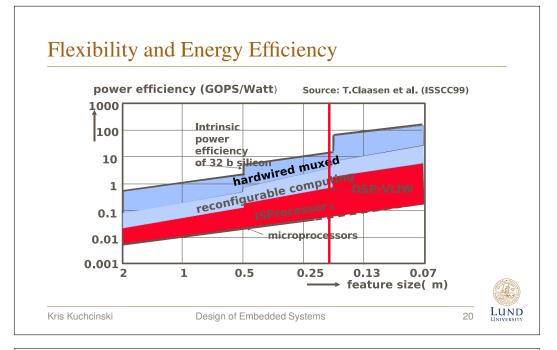
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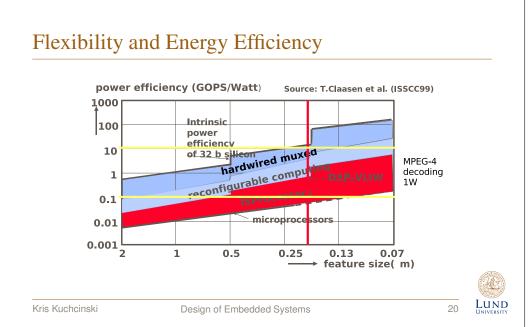
Design of Embedded Systems

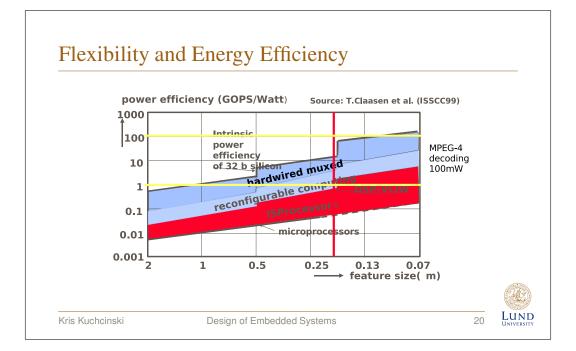


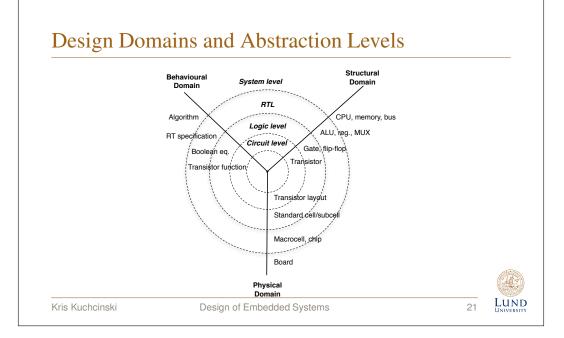
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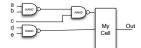




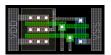


## **Design Domains**

- behavioral representations describe only circuit's function, for example
  - if clock=high then counter:= counter+1
- structural representations components and their interconnections, for example



• physical representations - either a geometrical layout or a topological constraint.

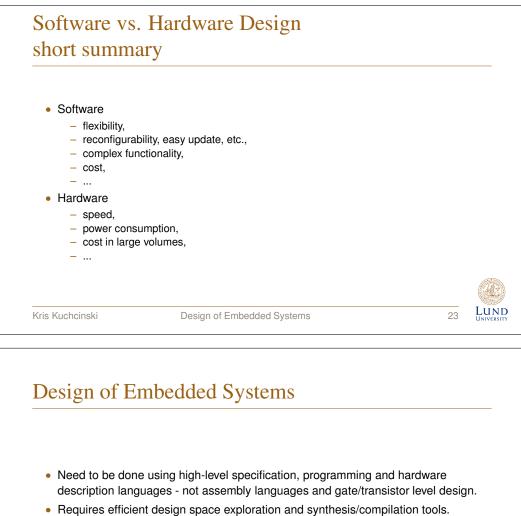




Design of Embedded Systems



22



- Different design requirements has to be taken into account, e.g., cost, performance, testability, quality of service, power consumption.
- · Multi-language design framework.

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Design of Embedded Systems



24

## Importance of High-Level Design Methods

System Verification Processing Speeds

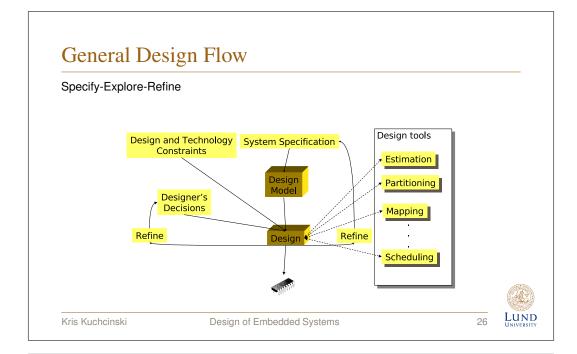
System implementation	Processing time (s/frame)		
Behavioral model	1 200 (20 min/frame)		
RTL model	144 000 (1.6 days/frame)		
Gate model	228 000 (2.6 days/frame)		
Gate model on hardware accelerator	1 200		
Rapid prototype	0.5		
Target hardware	0.05		

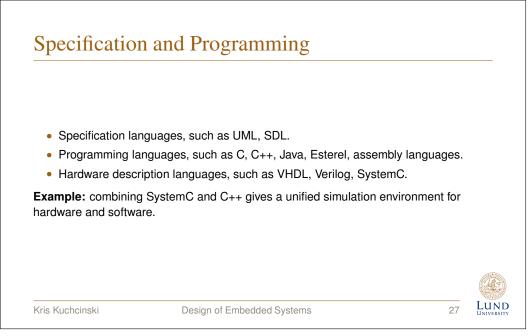
Source: Paul Clemente, Ron Crevier, Peter Runstadler "RTL and Behavioral Synthesis, A Case Study", VHDL Times, vol. 5, no. 47

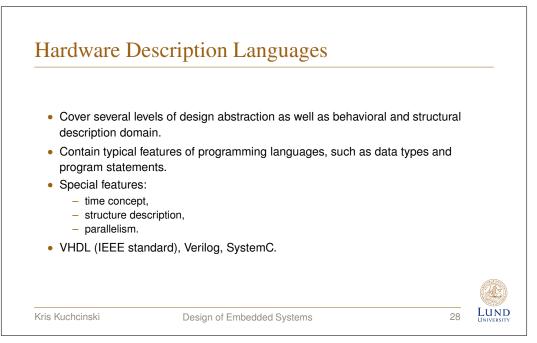
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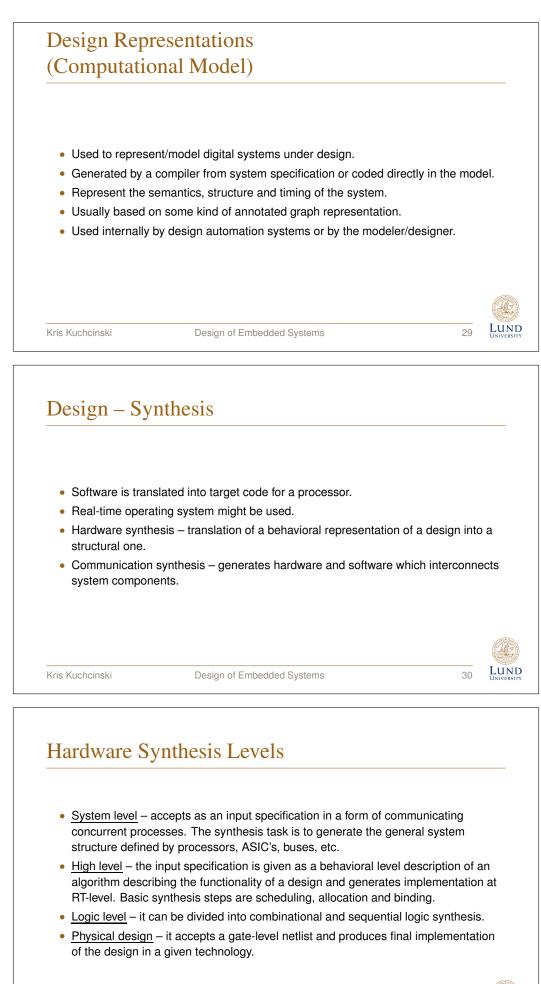
Design of Embedded Systems











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31

