REAL TIME SPECTROGRAM

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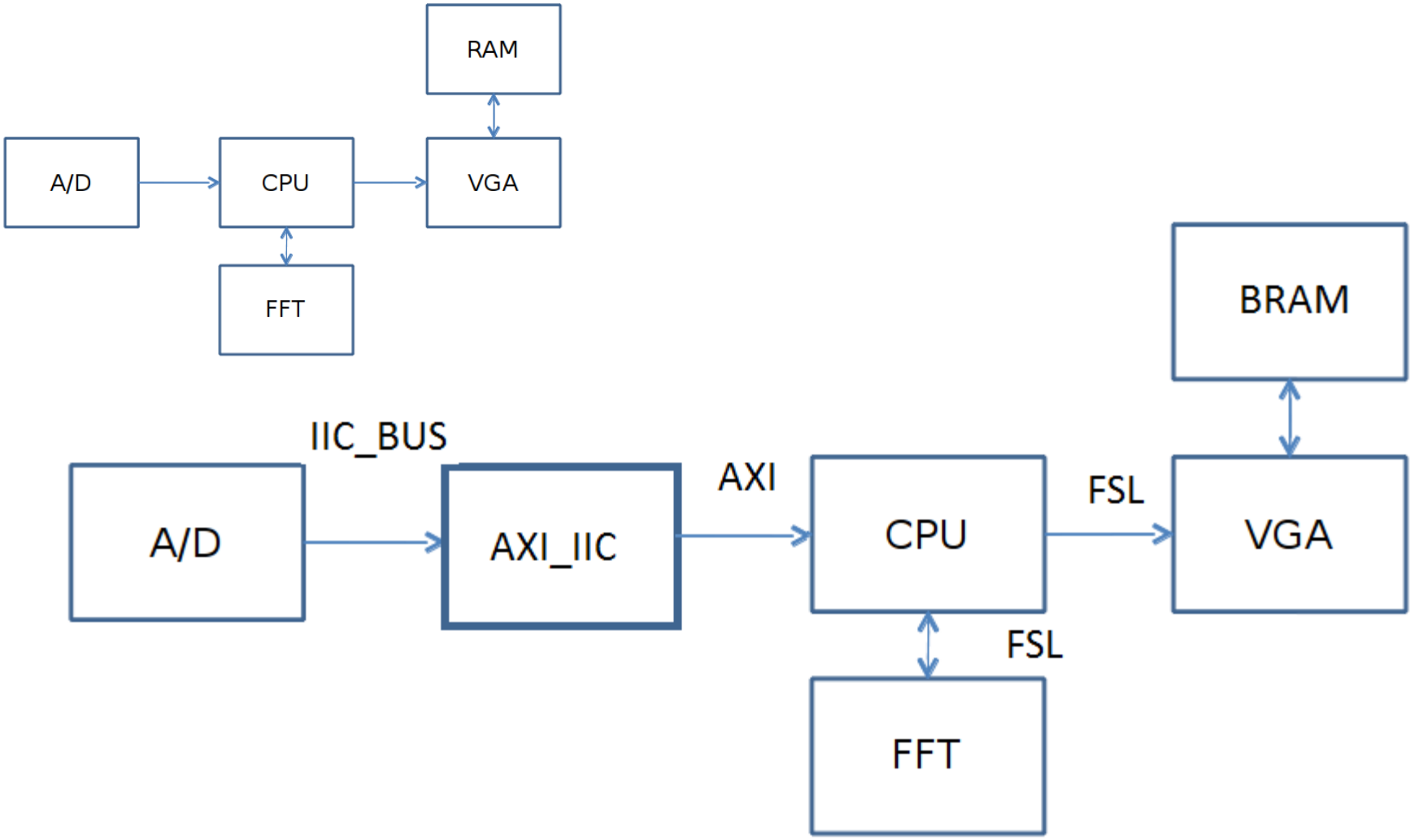
Architecture



FFT

- Implemented our own, too slow and too big

Solutions

- Found Core Generator
- AXI4-Stream to FSL converter

VGA Memory

- Tried to implement our own DMA but it was too slow.
  - A lot of work
  - page mode
  - Didn’t fit on the FPGA

Solution

  - BRAM (streched lower resolution)

A/D Hardware

- Pull up
- A/D converter works on positive Voltage only

Solution

- External pullups
- Added DC offset in hardware

A/D Software

- Communication
  - Our own IIC to fsl
  - Xilinx axi_IIC
  - Examples, high level
- Sample frequency

Solution

- AXI_IIC low level API
- Frequency still unsolved

Lessons

- Core generator
- Xilinx high level IIC Communication did not work
- Use premade IP cores

Conclusion

- Hardware
  - VGA and Block RAM
  - A\D Converter
  - FFT(256 points)
- Software
  - Communication controller

Questions?