

Camera Controller

Project Proposal Report - EDA385

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1 Introduction

The aim of this project is to implement an intelligent camera control system using a VGA camera module for video capture and a Nexys-3 board for video processing. The goal is that the system should be able to detect motion in the video stream and then track the moving objects while they are in the frame. If the project is successful and there is time left we have some stretch goals, these are:

1. Tracking with the camera to keep the moving object in the frame.
2. Face detection/recognition.
3. Complement the camera with speakers and microphone.

2 Identified Parts

The system is comprised of several parts, with the camera being the most obvious. To get images from the camera, a frame grabber will be needed. The high speed requirements, a pixel clock of ~ 14 MHz, demands that this is implemented in hardware. The other obvious part is the display. For this a VGA controller needs to be implemented. Also here it is not feasible to meet the strict timing requirements of the VGA standard with a software approach, so a hardware implementation is needed. For the actual motion detection a software based solution will be the first approach as there are libraries available that will make development easier. However, at least some parts of the motion detection algorithms will probably be implemented in hardware since the ~ 100 MHz MicroBlaze will probably not be powerful enough to do all the work at acceptable frame rates.

3 Specification

3.1 System Description

Figure 1 shows an overview of the system. The camera shall be connected to the Nexys board using the p-mod connectors on the board using the camera interface in figure 2. One p-mod connector will be used for data and one for control.

3.2 Camera Module

The camera module interface is shown in figure 2. All inputs are 2.8 V but should tolerate 3.3 V although lifetime may be affected. The outputs are 2.8 V. The input clock, $xclk$, needs to be between 10 and 48 MHz, with a typical value of 24 MHz. The clock duty cycle needs to be between 45% and 55%. The pixel color values are clocked out on $D(0:7)$ if $href$ is high. Pixel values are sampled at the rising edge of $pclk$.

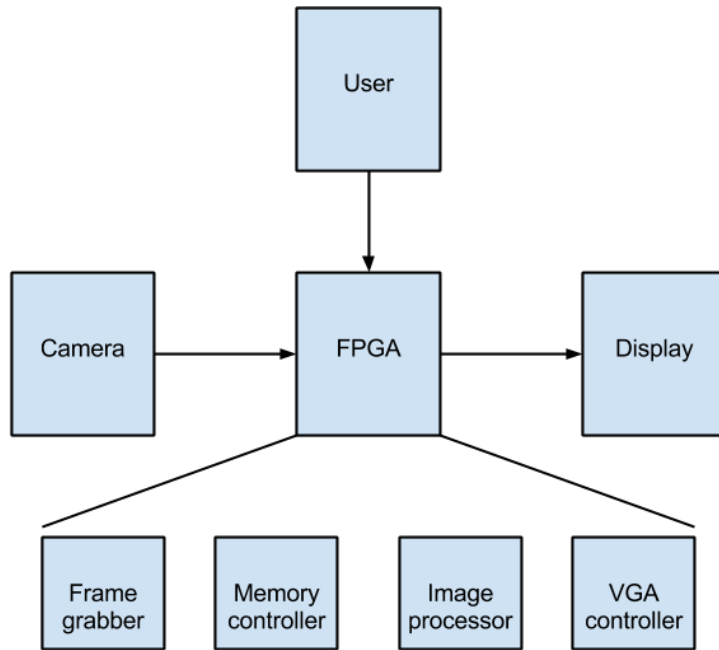


Figure 1: Rough Sketch of the System

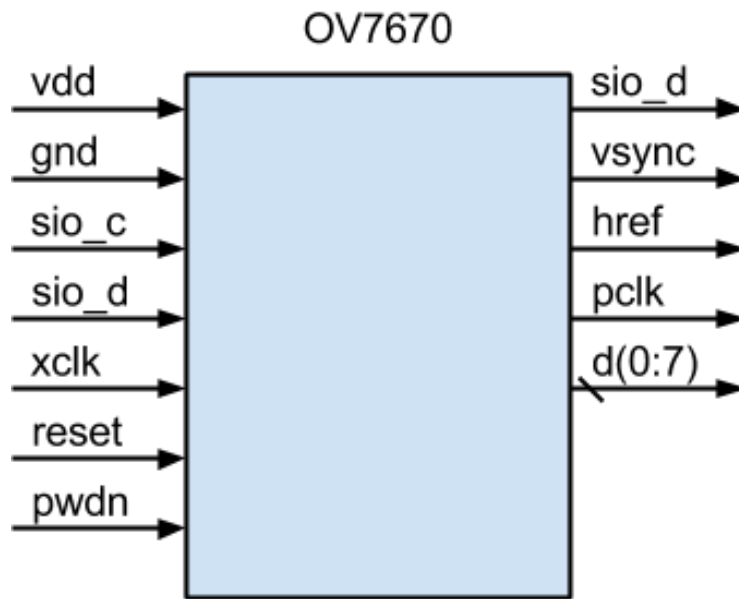


Figure 2: Camera Interface

3.3 Timing Requirements

The camera is specified at 640x480 resolution with a frame rate of 30 fps and 16 bit color depth. This would amount to $640 * 480 * 16 * 30$ b/s, or approx

18.5 MB/s of throughput. On the output side the most common VGA mode is 640x480@60 Hz although not at 16 bit color depth. Since the Nexys-3 board has a VGA-output with a simple 8 bit D/A-converter the goal is to output at, at least, that color depth, giving the same ~ 18.5 MB/s of throughput as on the input side.

3.4 VGA Output

The VGA output on the Nexys-3 consists of a simple resistor divider circuit that works in conjunction with the termination resistance of the VGA display to form the voltages required for the RGB signals. The levels of the signals are changed by means of ordinary digital outputs from the FPGA.

3.5 Memory Requirements

There will probably be a need for extra memory in the system to store the input from the camera. This data will be accessed and read by the output controller. With added features, this memory will be modified to the specifications.

4 Time Plan

This is the estimated time planning of the whole project. If there are any delays, the bonus features will be removed to accommodate.

Week	Date	Goal
0	8/9	Presentation of project report.
1	15/9	First implementation. Screen grabber, memory management and output.
2	22/9	Picture manipulation, performance testing. Support structure in C and/or VHDL.
3	29/9	Movement detection. Combine detection and picture output.
4	6/10	Add support for removing moving objects.
5	13/10	Sound sensitivity with microphone. Light sensitivity. Face recognition.
6	18/10	Demonstration.
7	27/10	Final report.