Computer Science
Faculty of Engineering
Lund University

Project Proposal
Two Player Tetris

Alexander Aulin, E07 (et07aa0)
Niklas Claesson, E07 (et07nc7)

Design of Embedded Systems
Advanced Course (EDA385)
September 17, 2012, Lund

Contents

1 General description

As project for this course a simple video game was thought to be fun and interesting to implement. Tetris was discussed but to make it a bit more interesting it was decided that a two player variant should be implemented. A sketch of the game can be seen in figure 1. The goal of the game is to collect as many complete lines as possible as fast as possible. Lowering the blocks faster will generate a higher score. To make it a two player game an extra layer of tiles will be added to the bottom of the other players screen when a player get a specific amount of lines at the same time.

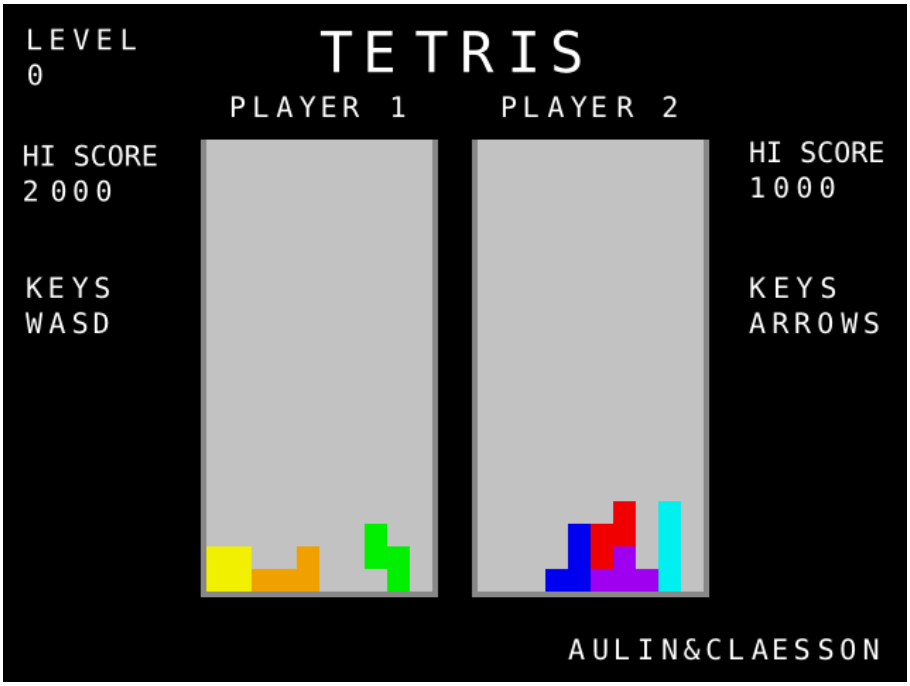

Figure 1: Text

Studying similiar implementations of 2-dimensional games made it clear that a sprite based graphics accelerator would be ideal for the purpose. The accelerator will be implemented as generic as possible to be useful for future game implementations. This means that all game logic will be stored as software procedures and all graphics, tiles and pallettes, will be loaded into memory on boot.

2 Specification

The peripheral units that is thought to be needed:

- Vga controller 640x480 pixels resolution 8-bit color
- Graphics accelerator
- Micron PSRAM for Microblaze/Sofware
- USB keyboard

The peripherals are connected via an AXI bus. An outline can be seen in figure 2. The PSRAM is thought to be used as memory for the Microblaze, at least for heap and stack. The PSRAM is huge, 16MB, and and will most likely not be filled.

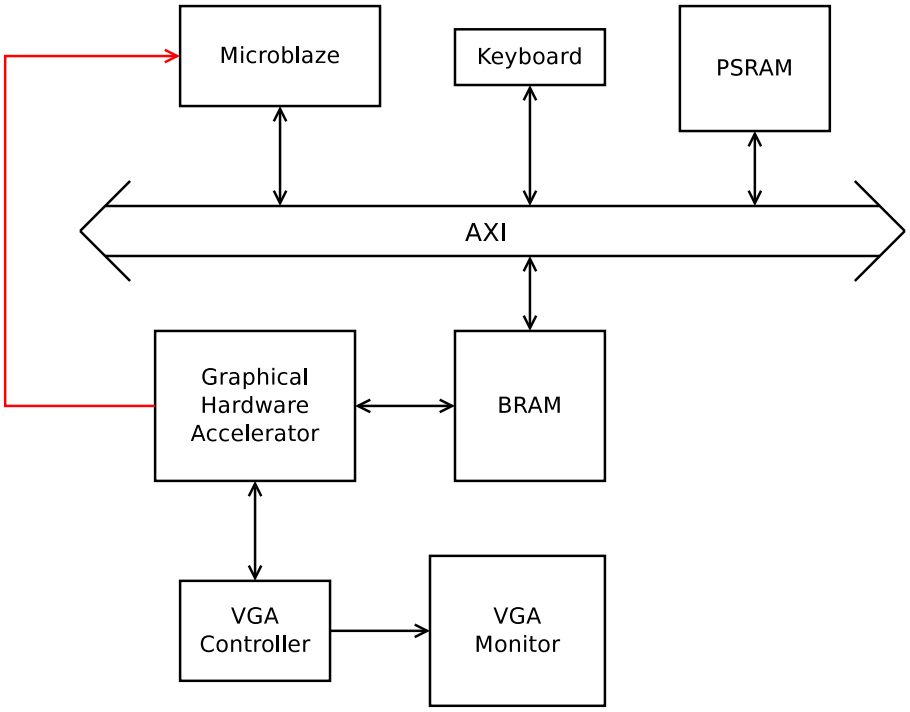

Figure 2: Text

These are the specifications of the grahpics accelerator:

- 16x16 spritesize
- 30x40 sprites matrix background
- 64 bitmaps
- 8 palettes with 4 colors
- Object memory, unspecified. 400?

A preliminary BRAM calculation:

$$
\begin{aligned}
size\_of(BGRAM) &= 30 \cdot 40 \cdot (log2(64) + log2(8)) = 10800\,bits \\
size\_of(ObjectRAM) &= 400 \cdot (\lceil log_2(40) \rceil + \lceil log_2(30) \rceil) + log_2(64) + log_2(8)) = 8000\,bits \\
size\_of(BitmapRAM) &= 64 \cdot (16 \cdot 16 \cdot log2c(4)) = 32768\,bits \\
sixe\_of(PaletteRAM) &= 8 \cdot (4 \cdot 8) = 256\,bits \\
size\_of(RowBuffer) &= 640 \cdot 8 = 5120\,bits \\
sum &= 10800 + 8000 + 32768 + 256 + 2 \cdot 5120 = 62064\,bits
\end{aligned}
$$

In total the needed BRAM for the accelerator together with instruction cache from the Microblaze is well below the total amount of available BRAM.

A preliminiary sketch of the hardware can be seen in figure 3.

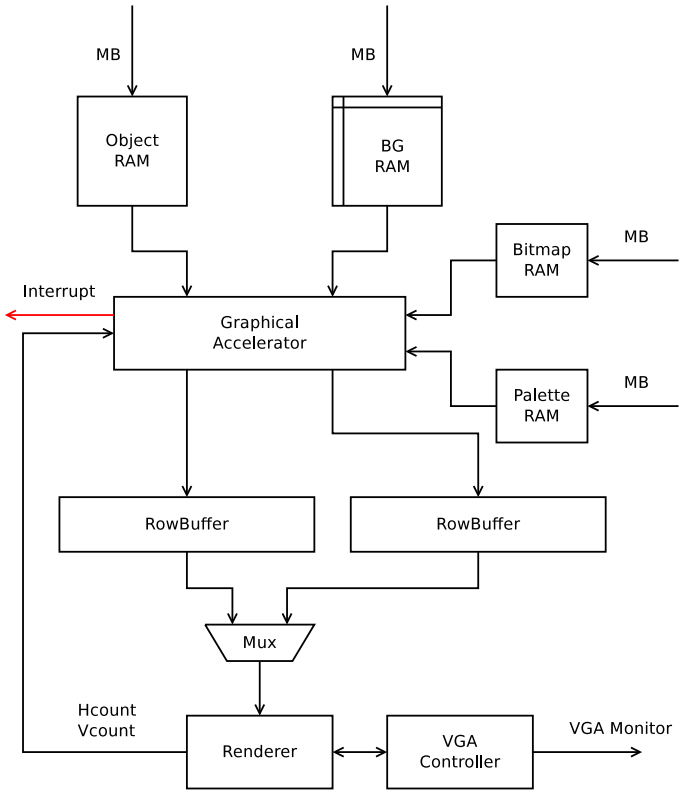

Figure 3: Text

3 Feasability Study

Projects made by last years students inspired and gave us many ideas. They also confirmed that this is a common way to implement a 2-dimensional graphics accelerator. Similiar games have been implemented by students from former years.

4 Work plan

In the beginning all focus will be on designing the hardware. When some work has been done on the hardware, like generating a MicroBlaze softcore with debug support, the software will be written in parallell to more hardware. During the last weeks there will be a lot of testing of the complete system and bugfixing. Every subsystem will of course be extensively tested whenever it is possible. In the final week the project report and last presentation will be written. The schedule can be seen in table 1.

Week 1	Week 2	Week 3	Week 4
Presentation 1	HW	HW	HW
Architecture	Artwork	SW	SW
			Testing

Week 5	Week 6	Week 7	Week 8
HW	Testing	Testing	Report
SW	Report	Report	
Testing		Presentation 2	

Table 1: Schedule