EDA385 – Project proposal presentation

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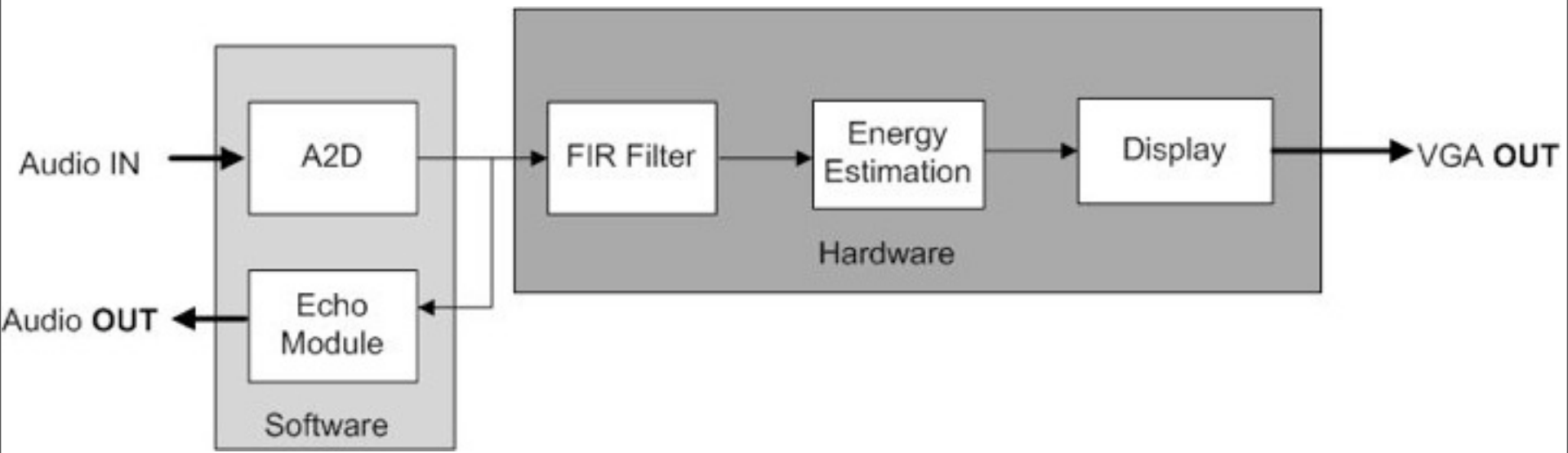
Audio visualizer with Echo

- FPGA will utilize VGA to output visualizations.
- Will employ the Nexys3 module.
- Sampled audio will be passed through a 10-bit FIR filter.
- Mean value of filtered audio data is calculated.
- PmodAMP1 will output the sound. (if

VHDL and C

- Echo generation (Implemented in C)
  - Sound buffer is required.
  - >32KiB fast memory will buffer the sound.
- FIR filtering (Implemented in VHDL)
  - FIR filter order will depend on the ADC resolution.
  - Time multiplexed FIR filter.
- VGA output driver 640x480 (VHDL)

Proposed block diagram



According to design (Visualizer)

- Audio enters from **IN**.
- **IN** audio passes through FIR filter.
- Filtered audio signal's mean value is estimated.
- Approximated mean values can be visualized on the display (VGA).

Echo

- Audio enters from **IN**.
- Audio samples are stored in a FIFO buffer.
- Delayed samples residing in FIFO bu are added to original **OUT** signal.

Time plan

Name	Jakub	Adeel	Usman
Week 1	Planning	Planning	Planning
Week 2	AD interfacing	VGA driver design	FIR filter design
Week 3	AD to FIR implementation	VGA driver implementation	AD to FIR implementation
Week 4	Echo implementation	Mean value implementation	Echo implementation
Week 5	Debugging and adiustments	Echo measurements	Report writing
Week 6	Report writing	Report writing	Report writing
Week 7	Presentation	Presentation	Presentation

Discussion

- A digital-to-analog converter might be needed to output the echo.

Questions?