EDA 385: FPGA-pod

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Original Vs. Actual Design

-The FPGA-pod: A music player built off of the Diligent NEXYS-2 board and add-on modules

- Necessary add-on modules include:

-1 PModAMP1 (Speaker/Headphone Amplifier)

-1 PModCLS (LCD Screen)

-1 PmodSD (SD Card Interface)

- Design:

LCD Screen (PModCLS)

Digilent Nexys2 Board

Speaker/Headphone Amplifier (PModAMP1)

SD Card Interface (PModSD)

Push-Button

Controls

&

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Reset

Proposed Vs. Actual Implementation



SD Card Communication

-SD Card: 3 pins for power, 6 pins for communication

- -SD Mode: operating mode for SD cards with no native host interface
 - -Data transfer made via synchronous byte oriented serial communication interface between SD card and host **SDC**
 - -Command frame: fixed length packet (6 bytes) is sent from host to card
 -Response from card can then be read after command
 - response time (NCR)



-Command response time (NCR) is 0-8 bytes



SD Controller

-Provides for reading data on SD card

-Originally implemented in hardware for speed but proved very difficult to debug

-Subsequently implemented in software

-Software drives individual pins on SD card

-SD card is first initialized

-Data can then be read using various commands

-PROBLEM: SD controller is too slow - each pin is driven directly via software

-Easily solved with more time to debug hardware controller

FAT File System

-SD card was formatted with FAT32 file system

- -Independent FAT file system library (software) used to read files and directories -Platform independent because no implementation of disk I/O
 - -Disk I/O implemented by user library can thus be instantiated on any kind of memory
- Operated using "black box" approach easy to use



Main functions

- * f_mount * f_open * f_close * f_read * f_opendir * f_readdir
- Register/Unregister a Work Area
- Open/Create a File
- Close a File
- Read File
- Open a Directory
- Read a Directory Item

WAVE File Format

-WAVE files are a specialized subset of RIFF files

-**ChunkSize:** file size in bytes (minus 8 bytes for ChunkID and ChunkSize fields) -New WAVE files (extended WAVE file format) do not follow this standard exactly -Most data stored in little-

endian standard endian big -PROBLEM: Data stored in little little-endian convention must big big be reversed before being used little -PROBLEM: New "extended wave little little file format" -- problems little little reading header to find data little

segment size



The "RIFF" chunk descriptor The Format of concern here is "WAVE", which requires two

sub-chunks: "fmt " and "data"

The "fmt " sub-chunk

describes the format of the sound information in the data sub-chunk

The "data" sub-chunk

Indicates the size of the sound information and contains the raw sound data

little

big

little

little

Audio Controller

-Little-endian WAVE file convention is handled here

 A splitter (hardware) rebuilds data in correct format for each audio channel before sending the data to the digital-to-analog converter

-At high sampling rate (CD quality – 44100 kHz) FIFO audio cue can be read faster than SD controller can write, producing cuts/loss in data

-Solution efforts:

 MicroBlaze clock frequency increased from 50 to 75 MHz via clock_generator IP-core (hardware)









Audio Controller Schematic DAC_sigma_delta_16_bits DAC_out Left Out> ck Splitter 151 FIFO sound Data(31:0) dout(31:0 udib_in(31:0) Left_Channel(15:0) lln(31:0) DAC_h(15:0) Wr_en Wr clk Right_Channel(15:0) r er r__cik full DAC_sigma_delta_16_bits Rd_en i er rd_dk DAC_out ck Right_Out) (UII)-121 -E) empty DAC_h(15:0) deb∎g ∂1 rst. debug(31:0) Clk 6k CLK_75M CLK_6000 CLK Bus 75M RST rst bus SIGI dcm150 RST_IN LOCKED_OUT CLK2X_OUT CLKN_IN CLK0_OUT 9 Lund University

Digital-to-Analog Converter

-Implemented in hardware

- -No external Digital-to-analog converter on PModAmp, used on-board DAC
- PROBLEM: Lack of traditional external DAC means lack of proper filtering
 - -PWM signals produced by DAC are linked directly to the inputs of PmodAMP

-Signals are not filtered properly

-A lot of noise exists in the audio output (PROBLEM - still unsolved)



User Interface

-Implemented almost entirely in software

-Push Buttons:

-Polling based

-software starts/pauses the current song or skips to next/previous song -Playlist:

-implemented in software through FatFS library

-Playlist/user interface initialized by scanning root directory for WAVE files

-Each entry in the playlist corresponds to a WAVE file in the root directory

-Song names are sent to LCD based on user push-button action

-LCD driven by UART (hardware) at 9600 bds







Lessons Learned & Conclusions

-Estimating time required to complete embedded systems projects, technical projects in general, is difficult and time required is easily underestimated

-Pros and cons must be considered when choosing to implement a design primarily in either hardware or software

 -For certain applications hardware implementation is a much better choice
-For other projects with demanding deadlines software implementation is sometimes easier to implement and debug

 Designing and successfully creating hardware in the real world is much more difficult, but also much more rewarding than simply designing hardware on paper

References

About SD, FATFS and Wave Files :

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- http://elm-chan.org/fsw/ff/00index e.html
- http://www.xilinx.com/support/documentation/ip

documentation/opb deltasigma dac.pdf

- http://www.sdcard.org/developers/tech/host controller/simple spec/ Simplified SD Host Controller Spec.pdf

How to use Xilinx EDK :

<u>http://www.labbookpages.co.uk/fpgas/edkHowTos/simple.html</u>
<u>http://courseware.ee.calpoly.edu/cpe-329/EDK_Resources.htm</u>



FPGA-pod

Questions?

